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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H03M 13/15 | A1

(11) International Publication Number: WO 00/28668

(43) International Publication Date: 18 May 2000 (18.05.00)

(21) International Application Number: PCT/US99/26554

(22) International Filing Date: 9 November 1999 (09.11.99)

(30) Priority Data:
60/107,879 9 November 1998 (09.11.98) US

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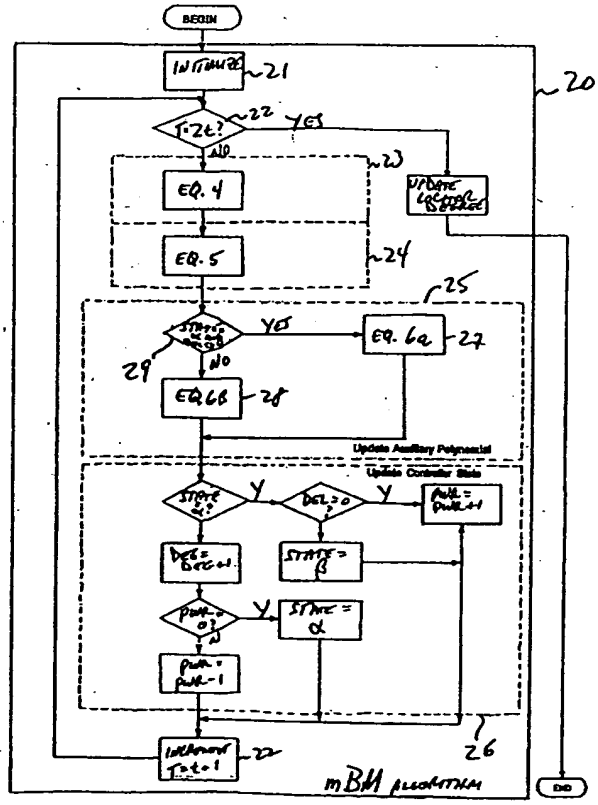
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: FORWARD ERROR CORRECTOR

(57) Abstract

A method for decoding an algebraic-coded message including determining a discrepancy indicator; determining an error locator polynomial according to a modified Berlekamp-Massey algorithm such that an uncorrectable message is detected; and producing a perceptible indication of the detected uncorrectable message. An apparatus includes storage devices, arithmetic components, and an uncorrectable message detector.



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FORWARD ERROR CORRECTOR

CROSS-REFERENCE TO RELATED APPLICATION

This patent application claims the benefit of the filing date of U.S. Provisional Patent Application Serial No. 60/107,879, filed November 9, 1998 and entitled FORWARD ERROR CORRECTOR, the entire contents of which are hereby expressly incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an apparatus for correcting errors present in stored or transmitted data; and, more particularly, to an apparatus for evaluating an error evaluator polynomial, an error locator polynomial and a differential polynomial which are used in correcting errors in the data encoded by using an algebraic code, such as a Reed-Solomon code.

2. Description of Related Art

Noise occurring during a process of transmitting, storing or retrieving data can in turn cause errors in the transmitted, stored or retrieved data. Accordingly, various encoding techniques, having the capability of rectifying such errors, for encoding the data to be transmitted or stored have been developed.

In such encoding techniques, a set of check bits is appended to a group of message or information bits to form a codeword. The check bits, which are determined by an encoder, are used to detect and correct the errors. In this regard, the encoder essentially treats the bits comprising the message bits as coefficients of a binary message polynomial and derives the check bits by multiplying the message polynomial $R(x)$ with a code generator polynomial $G(x)$ or dividing $R(x)$ by $G(x)$, to thereby provide a codeword polynomial $C(x)$. The code generator polynomial is selected to impart desired properties to a codeword upon which it operates so that the codeword will belong to a particular class of error-correcting binary group codes (see, e.g., S. Lin et al., "Error Control Coding: Fundamentals and Applications", Prentice-Hall, 1983).

One class of error correcting codes is the well-known BCH (Bose-Chaudhuri-Hocquenghen) codes, which include the Reed-Solomon ("RS") code. The mathematical basis of the RS code is explained in, e.g., the aforementioned reference by Lin et al. and also in Berlekamp, "Algebraic Coding Theory", McGraw-Hill, 1968, which is further referred to in U.S. Pat. No. 4,162,480 issued to Berlekamp. The aforementioned references are hereby incorporated by reference in pertinent part.

SUMMARY OF THE INVENTION

The invention herein provides a method and apparatus for decoding an algebraic-coded message. The method can include the steps of determining a discrepancy indicator, with the

discrepancy being between a calculated and a predicted value; determining an error locator polynomial using a selected class of error correction algorithms, such as, for example, a Berlekamp-Massey algorithm; and detecting an uncorrectable message using the selected error correction algorithm. The apparatus is composed of storage devices which can include recirculating storage devices; arithmetic components attached to the storage devices, the components operating over a Galois Field on selected contents of the storage devices; and an uncorrectable message detector, connected with the storage devices and the arithmetic components.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustration of a algebraic decoder according to the invention herein;

Figure 2 is a data flow diagram of a modified Berlekamp-Massey algorithm according to the invention herein;

Figure 3 is a block diagram illustrative of an exemplary embodiment of the present invention;

Figure 4 is a block diagram of a circular syndrome generator according to the present invention; and

Figure 5 is a block logic diagram of a logic register which can be used in the circular syndrome generator illustrated in Figure 4.

EXEMPLARY EMBODIMENTS OF THE INVENTION

The invention herein provides an apparatus for and a method of decoding algebraic codes, including BCH codes, and more specifically, Reed-Solomon codes, such that uncorrectable messages, or portions of received encoded data, are detected. Furthermore, the invention herein provides for a more area-efficient device implementation of the aforementioned method. For the purposes of illustration, the present invention will be described in terms of a subset of the BCH codes, namely Reed-Solomon (RS) codes.

The Reed Solomon (RS) encoding technique appends to each block of k user data symbols $2t$ redundancy symbols to create an encoded message block (where t represents the designed symbol error correcting capacity of the code). These $2t$ symbols, or elements, are selected from the Galois Field to be the roots of the generator polynomial. Therefore, there are $k+2t$ symbols in a RS-encoded message block. The entire message block is viewed as a polynomial and evaluated as a polynomial at some Galois Field element. The Galois Field element at which the polynomial is evaluated will be located at one roots of the generator polynomial that are used to create the RS code. The RS code views the n-bit symbols as elements of a Galois Field ($GF(2^n)$). A Galois field is a finite field, the elements of which may be represented as polynomials in a, where a is a root of an irreducible polynomial of degree n. The RS codeword consists of a block of n-bit symbols. Typically, $n = 8$ and the 8-bit symbols are

referred to as bytes. Constructing the Galois field $GF(2^n)$ requires a defining polynomial $F(x)$ of degree n. In addition, a primitive element β is chosen so that every nonzero element of $GF(2^n)$ is a power of β. The element β is not necessarily a root of $F(x)$.

A RS codeword C is viewed as a polynomial $C(x)$ and the redundancy symbols are chosen so that the roots of $C(x)$ include the roots of a generator polynomial $G(x)$ whose roots are $2t$ consecutive powers of β. The k user data symbols are viewed as the high order coefficients of a degree $k+2t-1$ polynomial, and the redundancy symbols are the coefficients of the remainder when this polynomial is divided by $G(x)$.

The process of corrupting the original code block $C(x)$ with errors can be viewed as adding an error polynomial $E(x)$ to $C(x)$. The resultant corrupted polynomial is known as the received polynomial $R(x)$, where $R(x)=C(x)+E(x)$. The v non-zero terms of the error polynomial contain the necessary information to completely reconstruct the original data $C(x)$, since each term corresponds to a symbol error location and magnitude.

Typically, RS decoding is a tripartite analysis: (1) syndrome computation; (2) solution of the error magnitude and locator polynomials; and (3) error location and magnitude estimation by respective implementations of, for example, a Chien search and the Forney algorithm. The syndromes contain error information divorced form the actual information that is intended to be analyzed for errors. The error locator polynomial provides information regarding the location of an error in the received signal, and the magnitude of the error can be determined by using both the magnitude and the locator polynomials.

The thrust of the RS error correction procedure is to reconstruct the error polynomial $E(x)$. Three polynomials are used to correct a received polynomial $R(x)$: $S(x)$, a syndrome polynomial; $\Lambda(x)$, an error locator (or error location) polynomial; and $M(x)$ an error magnitude polynomial. The syndromes are computed by evaluating the polynomial $R(x)$ at all roots of $G(x)$. These values are called syndromes and the syndrome polynomial $S(x)$ has these values as coefficients. The syndrome polynomial $S(x)$ is used to determine the existence of errors. The error locator polynomial $\Lambda(x)$ and the error magnitude polynomial $M(x)$ are computed from $S(x)$ by a key equation solver. The roots of the error locator polynomial $\Lambda(x)$ indicate positions in the data that are erroneous and both the error locator polynomial $\Lambda(x)$ and the error magnitude polynomial $M(x)$ are used to determine the true values of the erroneous data.

Two frequently-used RS error correction algorithms are the Berlekamp-Massey and the Euclid algorithms. The present invention recasts the Berlekamp-Massey algorithm such that the inversion process typically associated with the traditional Berlekamp-Massey (tBM) algorithm is eliminated. This is important because the inversion process includes determining the reciprocal of certain Galois field elements using division. Division is a time consuming arithmetic operation, the implementation of which can occupy needed component area in a device design. Therefore, the present invention can be particularly advantageous where area-efficient layout of a decoder device is desirable.

For further elaboration of the decoding process over Galois fields, including tBM, Chien searching, and Forney's Algorithm, see *Theory and Practice of Error Control Codes* by Richard E. Blahut (Addison-Wesley, 1983) which is incorporated by reference in pertinent part herein.

Figure 1 illustrates an implementation of this algorithm, in which a raw received signal 1 is directed to RS decoder unit 2 that is used to determine the error locations and error values. Signal 1 is provided to syndrome generator 3 and delay unit 4. In syndrome generator 3, the several syndromes 5 associated with the selected encoding are derived and transmitted to polynomial solver 5. The syndrome generator 3 calculates one syndrome for each of the $2t$ roots of $G(x)$. Polynomial solver 6 utilizes the syndromes to determine the coefficients of the error location polynomial $\Lambda(x)$ 7 and the coefficients of the error magnitude polynomial M(x) 8, which in turn are transmitted to error estimator 9. Estimator 9 calculates error signal 10 which is combined in summer 11 with delayed raw received input 12 to provide corrected data 13. Estimator 9 can include Chien search unit 14 which utilizes the error location polynomial $\Lambda(x)$ to search for the roots of the error locator polynomial, $r_1, \ldots, r_v$. Typically, the Chien search unit 14 employs a root finding technique which involves evaluating the error locator polynomial at all elements in the field $GF(2^n)$. The roots of the error locator polynomial $r_1, \ldots, r_v$ determine the error locations. The error values are then determined using Forney's algorithm unit 15. The delayed raw received input 12 is then corrected using the output of the Forney algorithm unit 15 and the raw received input which is transmitted by delay unit 4.

Traditionally, the Berlekamp-Massey (tBM) algorithm, which usually is realized in polynomial solver 6 can described by:

$$\Delta_r = \sum_{j=0}^{n-1} \Lambda_j^{(r-1)} S_{r-j} \tag{1}$$

$$L_r = \delta_r (r - L_{r-1} + (1-\delta_r) L_{r-1} \tag{2}$$

$$\begin{bmatrix} \Lambda^{(r)}(x) \\ B^{(r)}(x) \end{bmatrix} = \begin{bmatrix} 1 & -\Delta_r x \\ \Delta_r^{-1}\delta_r & (1-\delta_r)x \end{bmatrix} \begin{bmatrix} \Lambda^{(r-1)}(x) \\ B^{(r-1)}(x) \end{bmatrix} \tag{3}$$

$r=1,\ldots, 2t$ where $\delta_r = 1$ if both $\Delta_r \neq 0$ and $2L_{r-1} \leq r-1$, and otherwise $\delta_r = 0$. Then $\Lambda^{(2t)}(x)$ is the smallest-degree polynomial with the properties that $\Lambda_0^{(2t)}=1$, and

$$S_r + \sum_{j=1}^{n-1} \Lambda_j^{(2t)} S_{r-j} = 0 \qquad r = L_{2t}+1, \ldots, 2t$$

where initial conditions are $\Lambda^{(0)}(x)=1$, $B^{(0)}(x)=1$, and $L_0=0$.

It is evident that the inversion indicated in Eq. 3 requires a division operation.

The tBM algorithm is capable of properly decoding messages that can be decoded properly, however if there is an uncorrectable case which is detectable as being uncorrectable, the uncorrectable error may be undetected and the message decoded as if it did contain a correctable error. Many times, this improperly decoded message can create additional difficulties because the error may propagate through other processes in the system which employs tBM.

According to the invention herein, the modified Berlekamp-Massey (mBM) can be described by the following equations:

$$\Delta_i = \sum_{j=1}^{2t} \Lambda_{i-1}^{j-1} S^{i-j} \tag{4}$$

$$\Lambda_i = \Delta_{_} \Lambda_{i-1} + x \Delta_i B_{i-1} \tag{5}$$

$$B_i = \begin{cases} \Lambda_{i-1} & \Delta_{_} = \Delta_i \quad \text{(6a)} \\ x B_{i-1} & \text{(6b)} \end{cases}$$

where: $\Lambda \neq 0$

$B_0 = 1$

$\Delta_{-1} = 1$

Utilization of mBM for RS decoding can be advantageous because: (1) inversion is eliminated; (2) the control structure associated with the mBM algorithm is simplified relative to that of tBM; and (3) the termination conditions of tBM are modified such that if the code is uncorrectable, errors otherwise undetected by tBM, are detected and flagged as such.

One implementation of the mBM algorithm is as follows, as represented in Pascal code:

```
PROCEDURE FindLocatorBMC( VAR Syndrome,Locator:Polynomial; VAR OK:BOOLEAN );

VAR   Cnt: 0..MaxParitySyms-1;          { Loop Index                    }
      Pwr: 0..MaxParitySyms;            { Power Counter                 }
      State: (Alpha,Beta);              { State Machine State           }
      Deg:  INTEGER;                    { Degree                        }

      Del, Del0: Words;                 { Discrepancies                 }
      J:  INTEGER;                      { Del Index                     }

      TempPoly: Polynomial;             { Temporary Polynomial          }
      B     : Polynomial;               { Secondary Polynomial          }

BEGIN                                   { BEGIN FindLocatorBMC          }
  B.L. := 0; B.D [0] :=1;               { Initial B                     }
  Locator.L := 0; Locator.D [0] :=1;    { Initial Locator Poly          }
  Deg := 0; Pwr := 0; Del0 := 1;        { Cntr Initialization           }
  State := Alpha;                       { Machine State                 }
```

```
1     FOR Cnt := ParitySyms-1 DOWNTO 0 DO BEGIN      { Algorithm Loop          }

        Del := 0;                                    { Calculate Del           }
        FOR J := 0 TO LOCATOR.L DO
         IF Syndrome.L >= (ParitySyms-1-Cnt-J) THEN
         Del:= Add( Del, Multiply( Locator.D[J],Syndrome.D[ParitySyms-1-Cnt-J]));
5
        TempPoly :=                                  { Do Common Update        }
      PolyAdd( WordTimes( Locator, Del0 ), PolyShift( WordTimes( B, Del ), 1) );

        IF (State=Alpha) AND (Del<>0) THEN BEGIN     { Do Step A               }
    { writeln( stderr, '   B<-L' );}
            B := Locator;
            Del0 := Del
10          END                                      { Do Step A               }

        ELSE BEGIN                                   { Do Step B               }
    { writeln( stderr, '   B<-xB' );}
            B := PolyShift( B, 1 )
            END;                                     { Do Step B               }

15      IF State=Alpha  THEN BEGIN                   { State is Alpha          }
            IF Del=0 THEN Pwr := Pwr +1              { Increment Power Cntr}
            ELSE State := Beta                       { Update Next State       }
            END                                      { State is Alpha          }

        ELSE BEGIN                                   { State is Beta           }
            Deg := Deg+1;
            IF Pwr = 0  THEN State := Alpha          { Update Next State       }
20          ELSE Pwr := Pwr-1                        { Decrement Power Cntr    }
            END;                                     { State is Beta           }

        Locator := TempPoly                          { Update Locator          }
        END;                                         { Algorithm Loop          }

    Locator := PolyDenormalize( Locator, Deg);       {Update Locator Degree    }
25  OK := State=Alpha
    END;                                             { END  FindLocatorBMC     }
```

Often, when a forward error corrector properly detects an uncorrectable error, the existence of such an error usually is verified in a process by which the syndrome polynomials are recomputed. This approach can carry a substantial penalty relative to the process efficiency. Instead, an embodiment of the invention herein, having an improved control structure, verifies the existence of an uncorrectable error by checking the state of polynomial solver 6 at the end of the polynomial solving process.

Figure 2 exemplifies an embodiment of the process 20 implementing the aforementioned improved control structure in the context of the mBM algorithm recited in Equations 4, 5, and 6(a)-(b). Although the implementations described herein are postured for standard RS codes having a block length of, for example, 255 elements, such implementations also may be used in the context of extended Reed-Solomon codes which, in the example herein, would have 256

elements in the message block, i.e., have 256 elements in associated the Galois Field. It is desirable that, in step 21, the control variables DEG, PWR, and STATE, as well as error locator variables be initialized. It further is desirable to iterate through steps 23, 24, 25, and 26, 2t times, where *2t* is the number of syndrome polynomials to be evaluated, and *t* is the error correcting capability of the preselected code. Thus, at step 22, a counter tracking the number of completed iterations is employed. No additions or subtractions are needed in implementing the control variables, and only count up or down functions are used. Step 23 essentially implements Equation 4, in which the discrepancy value DEL, associated with a particular iteration, is determined. Similarly, step 24 implements Equation 5 in which the error locator polynomial is updated. In step 25, auxiliary polynomial B_i is updated according to Equation 6a in substep 27, or Equation 6b in substep 28, based on conditions determined by logic 26. For logic 29, it is desirable for both STATE = ALPHA AND DEL <> zero to direct the data flow via an implementation of Equation 6a in substep 27; otherwise substep 28 is used, implementing Equation 6b. Unlike the tBM algorithm where the polynomial shift term $(1-\delta_r)x$ in Equation 3 has been normalized, the mBM algorithm does not require normalization, avoiding an inversion/division operation. After the auxiliary polynomial is updated in step 25, the controller state is updated in step 26.

In general, the degree of the error locator polynomial is tracked by DEG, which is an upcounter descriptive of the true degree of the error locator polynomial and, thus, the number of errors in the message block. It also is desirable to construct an error locator polynomial who roots equate to the locations of an error. Essentially, process 20 attempts to synthesize a linear feedback shift register (LFSR) that predicts the values of the syndrome polynomial. Such a LFSR can be useful to find the error locations. Discrepancy value, DEL, then exposes a discrepancy between the predicted value of the syndrome polynomial, and the value of the current syndrome polynomial, and invites further processing to discover the location of the errors. PWR is a counter that keeps track of the number of times that the controller previously remained in STATE = ALPHA. It is desirable to have the STATE remain in control state BETA for a count equivalent to the number of times that STATE previously remained in control state ALPHA.

For the purposes of the invention herein, STATE can be used to (1) determine whether the error correction analysis ought to follow the flow of Equation 6a or 6b; (2) assist in determining whether the degree of the error locator polynomial ought to be increased; and (3) whether there exists an uncorrectable error. At the end of *2t* iterations, the value of STATE is once again determined at step 35. If the result is STATE = ALPHA, then the code is potentially valid; on the other hand, if STATE = BETA, then the error is flagged as uncorrectable. Potentially valid codes where STATE = ALPHA at step 35, also can be subjected to additional validation before being subsequently decoded. Indeed, in one subsequent operation, the number

of the error locator polynomial zeroes is compared with the value of DEG. A discrepancy between these two values also is indicative of an uncorrectable error.

Figure 3 is an exemplary embodiment of a polynomial solver using the mBM algorithm. Solver 50 can include syndrome generator register 51, recirculating syndrome register 52, first delay register 53, locator polynomial(Λ_i)register 54, auxiliary polynomial (B_i) register 55, second delay register 56, first multiplier 57, second multiplier 58, adder 59, Δ register 60, and Δ_ register 61. In another embodiment, syndrome generator 51 can be separate from solver 50. It is desirable for multipliers 57, 58, and adder 59 to operate on Galois Field elements. It also is desirable for register 51 to be logically arranged as a circular register or loop, such that particular register values can be used in a pre-defined sequence. Furthermore, it is desirable that registers 52, 54, and 55 be logically arranged as push-down stacks or FIFOs, and also that the values contained therein rotate synchronously. The error locator polynomial Λ_i are arranged in register 54 such that the least significant coefficient is at the top and the stack "grows down" as subsequent values are determined. It is desirable for the syndrome recirculating register 52 to operate such that the least significant coefficient is aligned with the bottom of the register, and the most significant with the top.

In the example of Figure 3, the error correcting capability, t, is selected to be 5 elements and, thus, syndrome register 51 is designed to employ $2t$, or 10, individual elements. Additionally, register 52 is selected to use t elements, register 54 is chosen to employ $t+1$ elements, and register 55 is intended to operate with t elements.

Initially, recirculating syndrome register 52 is pre-loaded with zeroes. As expressed in the aforementioned algorithm, an initial step involves calculating the discrepancy value DEL, which can be stored in register 60. A previous value for DEL, DEL0, is provided in register 61. To calculate the initial value for DEL, first syndrome value S_o is shifted into register 52, which value is received in first multiplier 57 along with the initial value of DEL, namely, DEL0,and the t-th value in locator polynomial register 54. After the indicated multiplication and creation of a DEL value, the values in registers 52, 54, and 55 are shifted down by one element. At first, the values in register 52 are zero, however, with subsequent clocking, successive values of S_i enter register 52 and are recirculated therethrough, for the clock cycles equivalent to $i=0$ to $2t-1$. As S_0 exits register 52 into first multiplier 57, corresponding values of Λ_0 are also transmitted to first multiplier 57 such that the value $S_0\Lambda_0$ is determined.

Concurrently with this calculation, value B_0 from register 55 is multiplied with then extant value for DEL in second multiplier 58 and the result is summed with $S_0\Lambda_0$ in adder 59 to produce the next value for DEL. This value of DEL is used to produce the next value for the error locator polynomial, namely, Λ_1. After this calculation, value S_0 is recirculated such that it bypasses first delay register 53 and re-enters recirculating register 52 at the top of the stack during the next clock cycle. During this next clock cycle, syndrome value S_1 is aligned, and multiplied, with Λ_0, and S_0 is aligned, and multiplied, with Λ_1. This process repeats such that

each of the syndrome values properly iterates through in the evaluation of the locator polynomial.

With the above information, a skilled artisan would be able to see the manner in which the values for error locator polynomial Λ_l and auxiliary polynomial B_l are determined. Where it is desired to rotate the values of B_l through register 55, second delay register 56 is bypassed. On the other hand, where it is desirable to utilize a previously calculated value of B_i, as indicated in the aforementioned algorithm, the value of B_l is directed into second delay register 56.

Continuing in Figure 3, calculation of the magnitude polynomial will be described. At the completion of $2t$ iterations as described above, register 52 will contain values S_4-S_8. In essence, determination of the magnitude polynomial can be modeled as $M(x) = \Lambda(x)\, S(x) \bmod x^{2t}$, in which the multiplication will be truncated after the $2t$ term. Indeed, only t terms need be determined under the assumption that no uncorrectable error was encountered. During the final iterations of the calculation of the error locator polynomial, register 52 is loaded with zeros such that, at the completion of $2t$ iterations, all storage locations in register 52 contain a zero value. After $2t$ iterations, the values in register 51 will be restored to their original positions, register 52 will contain all zero values and register 54 will contain the error locator polynomial, Λ_t. In am manner similar to the computation of the locator polynomial coefficients, the error magnitude coefficients are calculated iteratively. After t iterations, S_0 will be at the logical bottom of register 52 and Λ_0 at the logical bottom of register 54. At the completion of $t+1$ iterations, the product of multiplier 57 will be $S_0\ \Lambda_0$, the first term of the error magnitude polynomial. The output of adder 59 is directed to the logical top of register 55, which now will be used to build the magnitude polynomial. After iteration $t+2$, syndrome value S_0 will be aligned with locator value Λ_1, giving the product $S_0 \Lambda_1$; syndrome value S1 will be aligned with Λ_0, giving the product $S_1 \Lambda_0$; the summation of which giving $S_0 \Lambda_1 + S_1 \Lambda_0$, which is the second term of the error magnitude polynomial. This process will continue until all values of $M(x)$ are so determined. At iteration $2t$, all of the coefficients for the error magnitude polynomial will have been calculated. At this point, data flow of the error locator polynomial in register 54 and the error magnitude polynomial in register 55 can be directed out of solver 50.

Figure 4 illustrates one embodiment of a circular syndrome generator 70 that can be employed as register 51 in Figure 3, modified to accommodate an error correcting capability of $t=8$. Figure 5 is an embodiment 72 of one of the individual registers 71 in circular syndrome generator 70 in Figure 4. Although a circular syndrome generator is shown, it is by no means the only form of syndrome generator that can be employed as register 51.

The foregoing merely illustrates the principles of the invention, and it will thus be appreciated that those skilled in the art will be able to devise various alternative arrangements

which, although not explicitly described herein, embody the principles of the invention within the spirit and scope of the following claims.

What is claimed is:

1. A method for decoding an algebraic-coded message, comprising the steps of:

a. determining a discrepancy indicator;

b. determining an error locator polynomial according to an algorithm from a selected class of decoding algorithms wherein an uncorrectable message is detected; and

c. producing a perceptible indication of the detected uncorrectable message.

2. The method of claim 1 wherein the selected class of decoding algorithms is a Berlekamp-Massey algorithm.

3. The method of claim 2 wherein the Berlekamp-Massey algorithm is an iterative algorithm.

4. The method of claim 3 wherein the iterative algorithm further includes the step of evaluating the error locator polynomial for the presence of an uncorrectable message after an iteration.

5. An apparatus for decoding an algebraic-coded message, comprising:

a. a plurality of storage devices, selected ones of the storage devices being recirculating storage devices;

b. a plurality of arithmetic components operably connected with the plurality of storage locations, the arithmetic components being operative within a Galois field; and

c. an uncorrectable message detector, operably connected with the storage devices and the arithmetic components.

6. The apparatus of claim 5 wherein one of the recirculating storage devices is one of a recirculating syndrome polynomial storage device, a recirculating error location polynomial storage device, and an auxiliary coefficient storage device.

7. The apparatus of claim 5, further comprising a syndrome generator.

8. The apparatus of claim 7 wherein the syndrome generator is a circular syndrome generator.

9. The apparatus of claim 8 wherein the circular syndrome generator is a recirculating circular syndrome generator.

10. The apparatus of claim 6 wherein the one of a recirculating syndrome polynomial storage device, a recirculating error location polynomial storage device, and an auxiliary coefficient storage device, is an area-efficient device.

11. An apparatus for decoding an algebraic-coded message, comprising a circular syndrome generator.

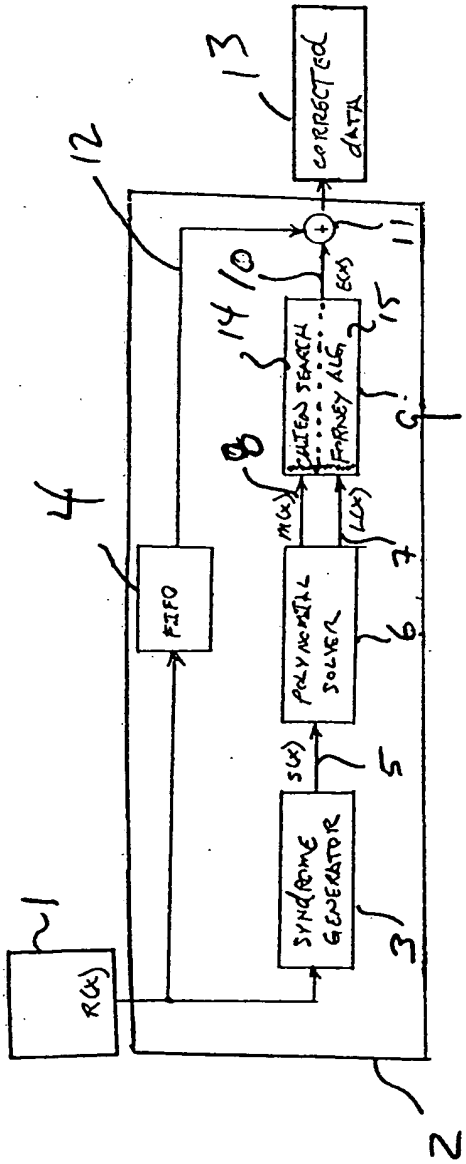
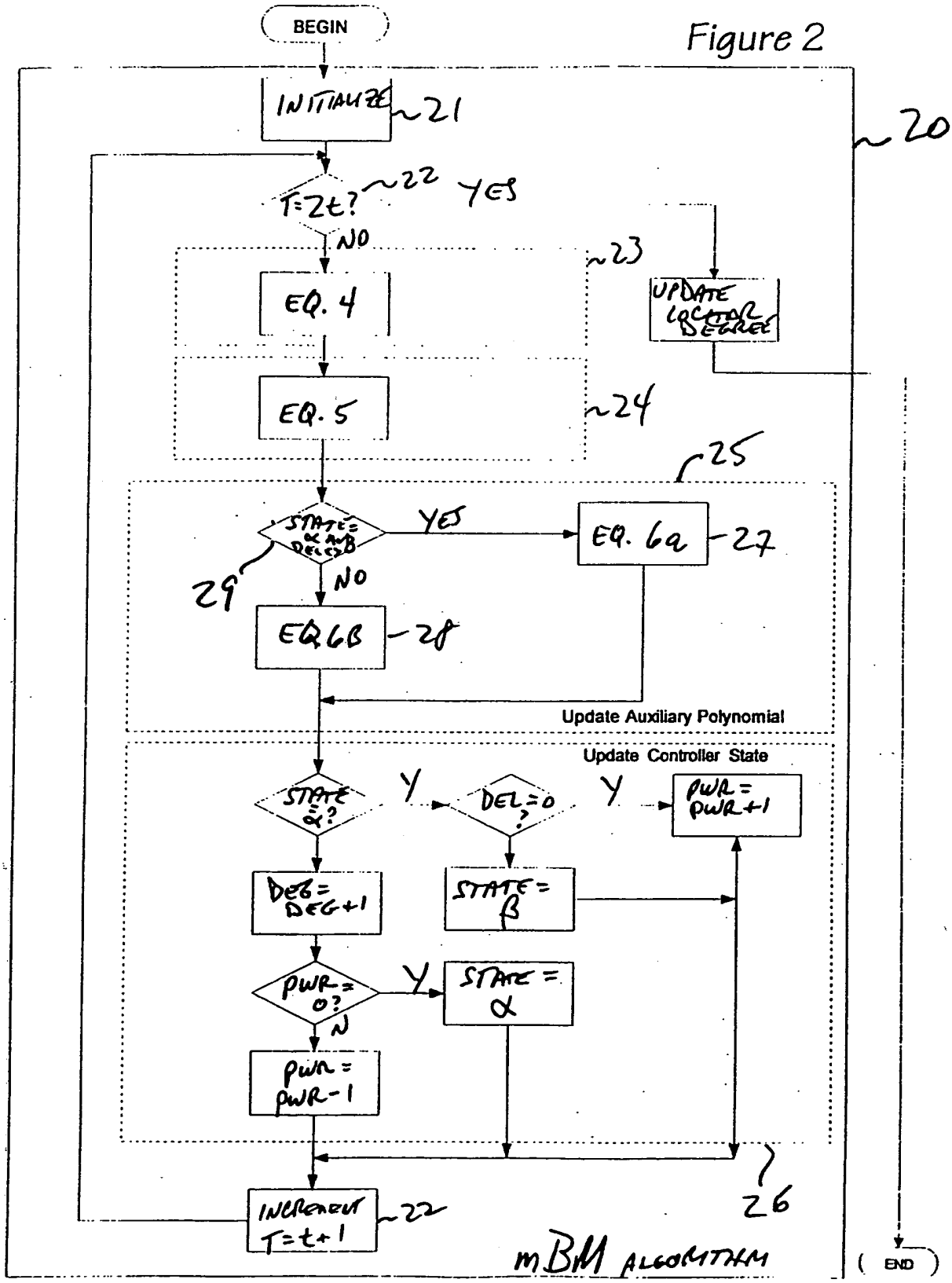

R(x)
FIFO
SYNDROME GENERATOR
S(x)
POLYNOMIAL SOLVER
M(x)
L(x)
EUCLIDEAN SEARCH FORNEY ALG.
EOS
CORRECTED DATA
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

FIGURE 1

Figure 2


BEGIN
INITIALIZE
21
20
T=2t?
22
YES
NO
23
EQ. 4
UPDATE LOCATOR DEGREE
EQ. 5
24
25
STATE = α AND DEL=0
YES
EQ. 6a
27
29
NO
EQ 6B
28
Update Auxiliary Polynomial
Update Controller State
STATE = α?
Y
DEL=0 ?
Y
PWR = PWR+1
DEG = DEG+1
STATE = β
PWR = 0?
Y
STATE = α
N
PWR = PWR-1
26
INCREMENT T=t+1
22
mBM ALGORITHM
END

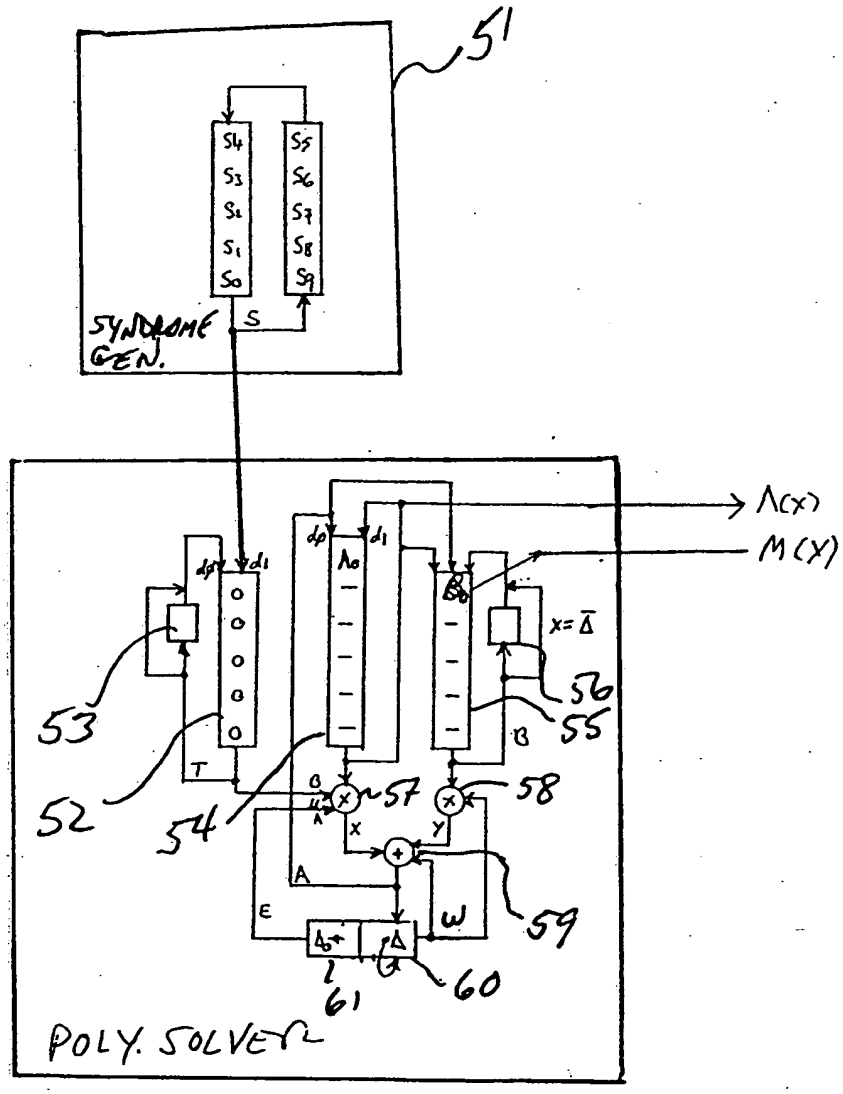

51
SYNDROME GEN.
S
$\Lambda(x)$
$M(Y)$
$x = \bar{\Delta}$
53
52
54
56
55
57
58
59
60
61
POLY. SOLVER

FIGURE 3

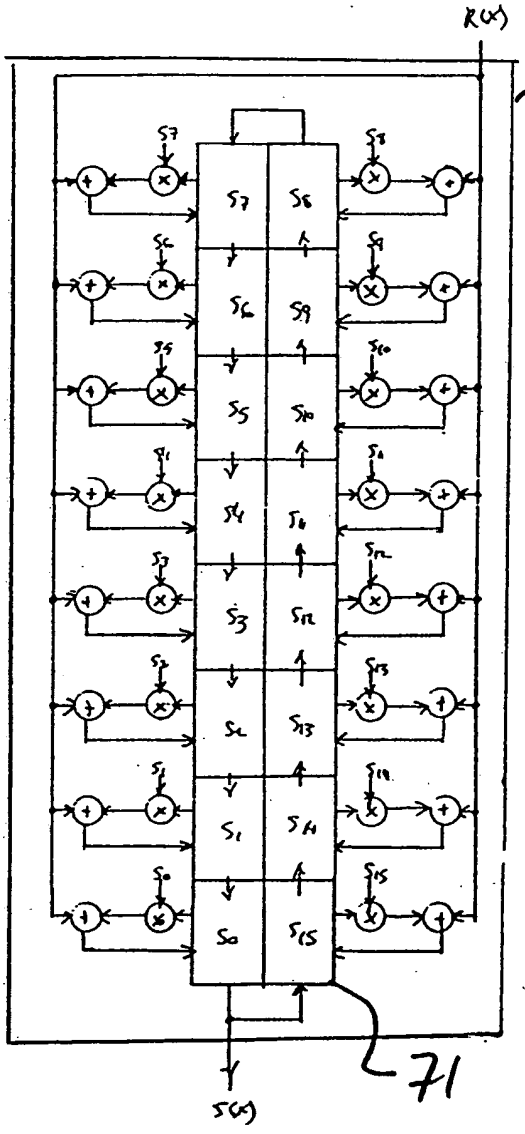


FIG. 4

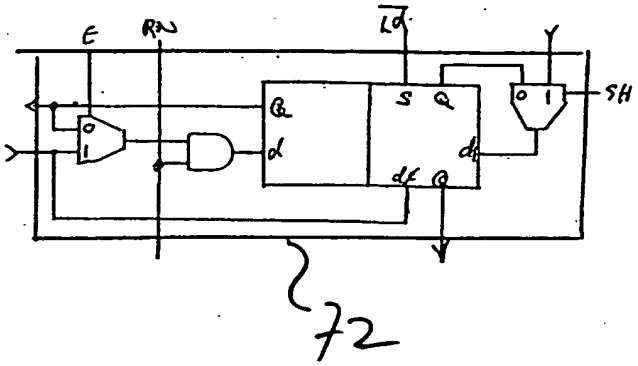


FIG. 5

INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/US 99/26554

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M13/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 099 482 A (CAMERON KELLY) 24 March 1992 (1992-03-24) page 10, column 2, line 23 - line 25 page 11, column 3, line 31 - line 34 page 11, column 4, line 53 - line 55 page 12, column 5, line 15 - line 33 figure 9	1-4
Y	BLAHUT E.R.: "theory and practice of error control codes" 1984 , ADDISON-WESLEY PUBLISHING COMPAGNY , LONDON XP002131806 page 176, paragraph 7.4 -page 178 page 191, paragraph 7.6 -page 193	1-4

-/--

[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
1 March 2000	15/03/2000

Name and mailing address of the ISA	Authorized officer
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Intern. nal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	TRIEU-KIEN TRUONG ET AL: "Inversionless decoding of both errors and erasures of Reed-solomon code" IEEE TRANSACTIONS ON COMMUNICATIONS, AUG. 1998, IEEE, USA, vol. 46, no. 8, pages 973-976, XP002131805 ISSN: 0090-6778	1

2

INTERNATIONAL SEARCH REPORT

information on patent family members

Intern al Application No
PCT/US 99/26554

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PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H04L 29/00 — A2

(11) International Publication Number: WO 00/28712

(43) International Publication Date: 18 May 2000 (18.05.00)

(21) International Application Number: PCT/US99/25675

(22) International Filing Date: 1 November 1999 (01.11.99)

(30) Priority Data:

60/106,441	30 October 1998 (30.10.98)	US
60/106,264	30 October 1998 (30.10.98)	US
60/106,427	30 October 1998 (30.10.98)	US
60/106,438	30 October 1998 (30.10.98)	US
60/106,439	30 October 1998 (30.10.98)	US
60/106,440	30 October 1998 (30.10.98)	US
Not furnished	29 October 1999 (29.10.99)	US

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(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: QUIGLEY, Thomas, J. [US/US]; 331 Sarah Lane, Lawrenceville, GA 30045 (US). DENNEY, Lisa, V. [US/US]; 1496 Willow Bend, Woodstock, GA 30188 (US). MIN, Jonathan, S. [US/US]; 6602 Notre Dame Drive, Buena Park, CA 90620 (US). JONES, Christopher, R. [US/US]; 4902 Neptune Avenue, Newport Beach, CA 92663 (US). SAMUELI, Henry [US/US]; 30926 Steeplechase, San Juan Capistrano, CA 92675 (US). LU, Fang [-/US]; 25 Arbusto, Irvine, CA 92606 (US). CHEN, Feng [CN/US]; 112 Remington, Irvine, CA 92620 (US). NAZARETH, Sean, F. [-/US]; 860 South Lee Marie Circle, Anaheim Hills, CA 92808 (US).

(74) Agent: CARTE, Norman, E.; Christie, Parker & Hale, LLP, P.O. Box 7068, Pasadena, CA 91109-7068 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

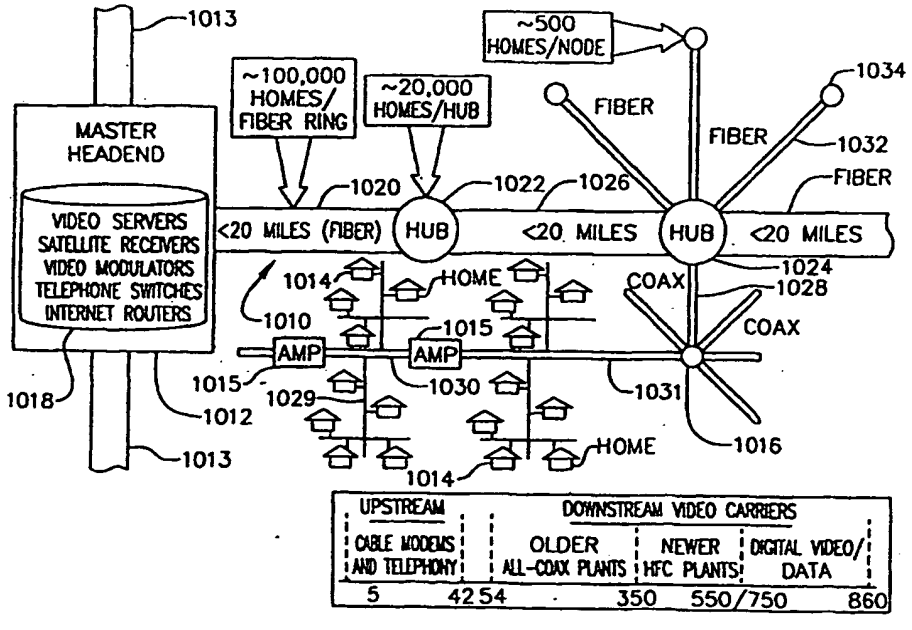
Published

Without international search report and to be republished upon receipt of that report.

(54) Title: CABLE MODEM SYSTEM

(57) Abstract

A method for communicating information includes allocating a time slot in a time division multiple access system for a transmission from a subscriber to a headend which is sufficient for only a first portion of a transmission. A second portion of the transmission is transmitted in other than the first time slot. Synchronization of a clock of the subscriber is enhanced with respect to a clock of the headend using a message transmitted from the headend to the subscriber which is indicative of an error in a subscriber transmission time with respect to the time slot. A feedback loop process is used to determine at least one of fractional symbol timing correction and carrier phase correction of a transmission from the subscriber to the headend. Quality of at least one channel is monitored and modulation is changed in response to changes in monitored channel quality. Information representative of parameters of received time division multiple access data is used to facilitate processing of the received time division multiple access data in a receiver. Filter coefficients are generated at the headend from a ranging signal which was transmitted from a subscriber to the headend and the filter coefficients are transmitted from the headend to the subscriber, where the filter coefficients are then used to compensate for noise in a transmission from the subscriber to the headend.



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CABLE MODEM SYSTEM

RELATED APPLICATIONS

This patent application claims the benefit of the filing date of the United States Patent Application filed October 29, 1999 as Attorney Docket No. 33539 and entitled CABLE MODEM SYSTEM; United States Provisional Patent Application Serial No. 60/106,264, filed October 30, 1998 and entitled HEADEND UPSTREAM MAC/PHY INTERFACE; United States Provisional Patent Application Serial No. 60/106,427, filed October 30, 1998 and entitled ROBUST TECHNIQUE FOR OPTIMAL UPSTREAM COMMUNICATION BETWEEN CABLE MODEM SUBSCRIBER AND A HEADEND; United States Provisional Patent Application Serial No. 60/106,438, filed October 30, 1998 and entitled SYSTEM FOR, AND METHOD OF, FRAGMENTING DATA PACKETS IN A CABLE MODEM SYSTEM; United States Provisional Patent Application Serial No. 60/106,439, filed October 30, 1998 and entitled CABLE MODEM SYSTEM; United States Provisional Patent Application Serial No. 60/106,440, filed October 30, 1998 and entitled NETWORK DATA TRANSMISSION SYNCHRONIZATION SYSTEM AND METHOD; United States Provisional Patent Application Serial No. 60/106,441, filed October 30, 1998 and entitled BURST RECEIVER SYSTEM, the entire contents of all of which are hereby expressly incorporated by reference.

FIELD OF THE INVENTION

The present invention relates generally to communication systems. The present invention relates more particularly to a cable modem system wherein information is communicated between a plurality of cable modems and a cable modem termination system.

BACKGROUND OF THE INVENTION

The desired solution for high speed data communications appears to be cable modem. Cable modem is capable of providing data rates as high as 56 Mbps, and is thus suitable for high speed file transfer, video teleconferencing and pay-per-view television. Further, cable modems may simultaneously provide high speed Internet access, digital television (such as pay-per-view) and digital telephony.

Although cable modem is a shared access system, wherein a plurality of subscribers compete for bandwidth over a common coaxial cable, any undesirable reduction in actual data rate is easily controlled simply by limiting the number of shared users on each system. In this manner, each user is assured of a sufficient data rate to provide uninterrupted video teleconferencing or pay-per-view television, for example.

SUMMARY OF THE INVENTION

The present invention specifically addresses and alleviates the above-mentioned deficiencies associated with the prior art.

According to an aspect of the invention a modem communicates with a cable transmission system. The modem requests an amount of bandwidth on the cable system to transmit data.

The modem receives a grant of an amount of bandwidth to transmit data in response to the request. The modem compares the requested amount of bandwidth with the granted amount of bandwidth. Responsive to the comparison, the modem fragments the data to be transmitted into a plurality of segments if the requested amount is larger than the granted amount. One of the segments is no larger than the granted amount. Responsive to the grant, the modem transmits all the data to be transmitted to the cable system if the requested amount is no larger than the granted amount and transmits only the one segment to the cable system if the requested amount is larger than the granted amount.

In another aspect, the present invention includes a method for facilitating communications between a plurality of cable modems and a cable modem termination system. The method comprises transmitting a request from the cable modem to the cable modem termination system. The request is a request to transmit a data packet from the cable modem to the cable modem termination system. A time slot for transmitting the data packet from the cable modem to the cable modem termination system is allocated, optionally by the cable modem termination system. Information representative of the time slot is then transmitted, optionally by the cable modem termination system, to the cable modem. The cable modem then transmits the data packet from the cable modem to the cable modem termination system within the allocated time slot.

Transmitting the data packet from the cable modem to the cable modem termination system within the time slot mitigates collisions between data packets which are transmitted by different cable modems to the cable modem termination system at the same time and upon the same frequency channel.

In another aspect, the present invention includes an apparatus and method for synchronizing upstream communications between a plurality of cable modems and a cable modem termination system (CMTS). A first message representative of a frequency of a clock of the cable modem termination system is generated, particularly by the cable modem termination system. Similarly, a second message representative of a slot timing offset of a selected one of the cable modems with respect to the clock of the cable modem termination system is generated, again particularly by the cable modem termination system. The first and second messages are transmitted to the selected cable modem. Frequency synchronization of the clock of the selected cable modem is enhanced with respect to the cable modem termination system utilizing the first message. The slot timing offset of the clock of the cable modem with respect to the clock of the cable modem termination system is compensated for using the second message. This process is repeated, as necessary, for each cable modem which is to communicate with the cable modem termination system.

In another aspect, the present invention includes an apparatus and method for rapidly acquiring data packets in a receiver such as that of a cable modem termination system. The method generally comprises determining fractional symbol timing correction by a feedback loop process, determining carrier phase correction by a feedback loop process and determining fine amplitude by a conventional coherent estimation process.

Optionally, the amplitude of the input to the fractional symbol timing correction circuit and/or the input gain to the carrier phase correction circuit may be adjusted so as to be within the

optimal operational range of the fractional symbol timing correction circuit and/or the carrier phase correction circuit via the use of phase detector gain boosting logic, wherein a sensor senses the amplitude of the signal input to the fractional symbol timing correction circuit and/or the carrier phase correction circuit and the amplitude of the signal is then modified so as to be within the optimal range.

Optionally, timing recovery may be accelerated by utilizing two out-of-phase, e.g., 180 degree out-of-phase, sampling timing signals such that one of the two sampling timing signals will always be located sufficiently distant from a null point in a binary input sequence as to enhance timing recovery.

Another aspect of the present invention is a method for communicating modulated information from a plurality of cable modems to a cable modem termination system in a way that enhances the robustness of the upstream channels. One way is to monitor upstream channels for at least one modulation parameter which is indicative of channel quality and adjusting the modulation in response to the channel quality parameter.

Another way is to vary the symbol rate of information transmitted over a channel in a near-continuous manner by varying at least one of the upper and lower bounds.

Another way is to monitor the upstream channels and to use fine carrier frequency agility and/or variable symbol rate to facilitate dynamic channel allocation so as to communicate only within channels having quality which is above a predetermined threshold.

According to another aspect of the present invention, slot timing information and/or data-type information is transmitted from a MAC to a burst receiver so as to facilitate processing of upstream data packets by the burst receiver in an efficient and reliable manner. Error information is transmitted from the burst receiver to the MAC. The error information is used by the MAC to facilitate spectrum management which enhances the data rate and/or reliability of upstream communications.

In an aspect of the invention, noise is abated in a cable system. The cable system has a headend and a plurality of user terminals interconnected by a cable that has a single downstream transmission path from the headend to each of the user terminals and a plurality of upstream transmission paths from each of the user terminals to the headend. A notch filter at the headend is adjusted to reject one or more bands of common noise. A feedback equalizer (FBE) at the headend compensates for the distortion caused by the notch filter. Afterwards, a ranging signal is received at the headend from each user terminal and feedforward equalizer coefficients corresponding to the transmit equalizer coefficients for each user terminal are generated from the ranging signals. The feedforward equalizer (FFE) coefficients are transmitted to the respective user terminals, where they are applied to a transmit equalizer filter to compensate for individual noise at the respective user terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects and advantages of the present invention will be more fully understood when considered with respect to the following detailed description, appended claims and accompanying drawings wherein:

Data Packet Fragmentation in a Cable Modem System

FIG. 1 is a schematic diagram showing the fragmentation of a data packet of a cable modem into first and second portions thereof, wherein the first portion of the data packet is placed in a first time slot allocated by the cable modem termination system and the second portion of the data packet is placed in a second time slot allocated by the cable modem termination system;

FIG. 2 is a schematic diagram of a hybrid fiber coaxial (HFC) network showing typical pathways for data transmission between a headend (which contains the cable modem termination system) and a plurality of homes (each of which contain a cable modem);

FIG. 3 is a simplified block diagram of a cable modem system wherein a line card or cable modem termination system (CMTS) is disposed at a headend and a cable modem is disposed within a home;

FIG. 4 is a schematic diagram showing the formation of an exemplary MAP which is transmitted by the cable modem termination system (CMTS) to all of the cable modems on a particular channel so as to facilitate communication of the cable modems with the cable modem termination system according to a time division multiple access (TDMA) protocol which avoids collisions among data packets from different cable modems;

FIG. 5 is a schematic diagram showing the formation of frames by a cable modem in response to receipt of a MAP, such as that shown in FIG. 4;

FIG. 6 is a flowchart showing the operation of the cable modem termination system in separating high priority requests and low priority requests received from cable modems;

FIGs. 7 and 8, taken together, define a flowchart showing the operation of the cable modem termination system in granting requests from cable modems to transmit data from the cable modems to the cable modem termination system;

FIGs. 9 and 10, taken together, define a block diagram of that portion of the cable modem termination system which receives requests from the cable modems and which generates MAPs in response to these requests and also shows a plurality of cable modems which receive the MAPs and which generate frames in accordance with the MAPs;

FIG. 11 is a schematic diagram of a complete packet according to the present invention, which is used to transmit data from a cable modem to a cable modem termination system;

FIG. 12 is a schematic diagram of a plurality of complete packets according to the present invention, used to transmit data on a concatenated basis from a cable modem to the cable modem termination system;

FIG. 13 is a schematic diagram of a plurality of packet fragments transmitted from a cable modem to the cable modem termination system, wherein the packet fragments form, in composite, a complete packet;

FIG. 14 shows the format of one of the packets of FIG. 13 in further detail;

FIGs. 15 and FIG. 16, taken together, define a table providing further detail of the fragmentation format of a frame which incorporates a packet;

FIGs. 17 and 18, taken together, define a flowchart showing how a cable modem and a cable modem termination system cooperate to facilitate the fragmentation of packets by the cable modem for transmission to the cable modem termination system;

FIG. 19 is a flow chart illustrating the fragmentation process;

FIG. 20 is a modification of FIG. 2 adapting the invention to wireless transmission;

FIG. 21 is a modification of FIG. 3 adapting the invention to wireless transmission; and

FIG. 22 is a schematic diagram of a single integrated circuit chip adapted to practice the invention.

Network Data Transmission Synchronization System and Method

FIG. 1 is a block diagram showing a cable modem termination system and an exemplary cable modem communicating with one another via a cable plant;

FIG. 2 is a block diagram showing the cable modem termination system and cable modem of FIG. 1 and further detail;

FIG. 3 is a block diagram showing the cable modem termination system of FIG. 1 in further detail;

FIG. 4 is a block diagram showing the cable modem of FIG. 1 in further detail;

FIG. 5 is a table showing an example of loop filter coarse coefficients and fine coefficients which provide specified bandwidths at the listed update rates;

FIG. 6 is a flowchart showing the software level synchronization control of a cable modem; and

FIG. 7 is a flowchart showing the hardware level synchronization control of a cable modem;

FIG. 8 shows the contribution of propagation delay and process delay to the slot timing offset.

Burst Receiver for Cable Modem System

FIG. 1 is a simplified block diagram showing the use of a fractional symbol timing loop, a carrier phase correction loop and a conventional amplitude estimator to enhance the rate at which acquisition of data packets is performed in a burst receiver of a cable modem termination system or the like;

FIG. 2 is a schematic diagram of a hybrid fiber coaxial (HFC) network showing typical pathways for data transmission between the headend (which contains the cable modem termination system) and a plurality of homes (each of which contain a cable modem);

FIG. 3 is a simplified block diagram of a cable modem system wherein a line card which defines a cable modem termination system (CMTS) is disposed at the headend and a cable modem is disposed within a representative home;

FIG. 4 is a block diagram showing a cable modem termination system and a representative cable modem communicating with one another via a cable plant;

FIG. 5 is a block diagram showing the cable modem termination system and cable modem of FIG. 3 in further detail;

FIG. 6 is a block diagram showing the cable modem termination system of FIG. 3 in further detail;

FIG. 7 is a block diagram showing the cable modem of FIG. 3 in further detail;

FIG. 8 is a table showing an example of loop filter coarse coefficients and fine coefficients which provide specified bandwidths at the listed update rates;

FIG. 9 is a flowchart showing the software level synchronization control of a cable modem; and

FIG. 10 is a flowchart showing the hardware level synchronization control of a cable modem;

FIG. 11 shows the contribution of propagation delay and process delay to the slot timing offset.

FIG. 12 is a block diagram showing the interrelationships of the burst transmitter, subscriber medium access control (MAC) and receiver of the cable modem with the burst receiver, medium access control (MAC) and transmitter of the cable modem termination system;

FIG. 13 is a block diagram showing the interconnections of the burst receiver, medium access control (MAC) and transmitter downstream modulator within a cable modem termination system;

FIG. 14 shows a continuous data stream, such as that which may be received by a conventional continuous receiver;

FIG. 15 shows a plurality of data bursts separated by guard bands, such as those transmitted by cable modems to a cable modem termination system according to time division multiple access (TDMA);

FIG. 16 shows in further detail an exemplary data burst of FIG. 15;

FIG. 17 shows the QPSK preamble of FIG. 16 in further detail;

FIG. 18 is a block diagram of a contemporary phase locked loop;

FIG. 19 is a block diagram of a fractional symbol timing loop in a typical digital receiver, wherein the matched filter is within the loop;

FIG. 20 is a block diagram of the fractional symbol timing loop of the present invention, wherein the matched filter has been moved outside the fractional symbol timing loop;

FIG. 21 is a block diagram showing a burst receiver having a fractional symbol timing loop, a carrier phase correction loop and an amplitude estimator so as to effect fast acquisition of data packets;

FIG. 22 is a block diagram showing a burst receiver having a fractional symbol timing loop, a carrier phase correction loop and an amplitude estimator, wherein the matched filter has been moved outside of the fractional symbol timing loop, so as to mitigate undesirable delays within the fractional symbol timing loop caused by the matched filter. The minimum delay in the loop is essential for fast burst acquisition using the feedback loop architecture. An open-loop resampler is required to resample the input signal relative to the symbol rate, in dependent of the ADC sample clock rate;

FIG. 23 is a block diagram of a phase detector gain boosting logic circuit wherein the amplitude of a signal input to a phase detector is monitored by a sensor and the amplitude of the signal to the low pass filter of the loop is controlled by the output of the sensor; and

FIG. 24 is a timing diagram showing the use of a single contemporary clock signal to provide timing for a sampling circuit contemporary clock signal (FIG. 24-A) to provide timing for a sampling circuit and also showing the use of two out-of-phase clock signals (FIG. 24-B), wherein and also showing the use of two out-of-phase clock signals, wherein one of the two out-of-phase clock signals will always have a timing relationship relative to the input binary signal to effect sampling of the input binary signal.

Robust Techniques for Optimal Upstream Communication

FIG. 1 is a block diagram of a prior art technique showing a plurality of contemporary demodulators coupled to demodulate data which is input from a transmission medium such as a fiber optic or coaxial cable and which is coupled to provide the demodulated data as an output thereof;

FIG. 2 is a block diagram of one aspect of the present invention, showing a monitoring circuit coupled to monitor a plurality of upstream channels for at least one parameter which is indicative of channel quality;

FIG. 3 is a block diagram of a prior art upstream burst receiver and medium access control (MAC) showing modulated data input from a transmission medium, such as a coaxial cable, to the upstream burst receiver and showing digital data output from the MAC;

FIG. 4 is a block diagram showing an aspect of the present invention;

FIG. 5 is a chart showing RS coding gain for various T's using 16-QAM with K equals 64 bytes;

FIG. 6 is a schematic drawing providing an example of fine frequency agility, wherein the frequency spectrum is divided into a plurality of closely spaced channels;

FIG. 7 is a flowchart showing dynamic channel allocation control flow; and

FIG. 8 is a flow chart showing CMTS dynamic channel allocation control flow.

Cable Modem Termination System Upstream MAC/PHY Interface

FIG. 1 is a simplified block diagram showing the MAC/PHY interface of the present invention;

FIG. 2 is a block diagram showing a plurality of contemporary demodulators coupled to demodulate data which is input from a transmission medium such as a fiber optic or coaxial cable and which is coupled to provide the demodulated data as an output thereof;

FIG. 3 is a block diagram of one aspect of the present invention, showing a monitoring circuit coupled to monitor a plurality of upstream channels for at least one parameter which is indicative of channel quality;

FIG. 4 is a block diagram of a prior art upstream burst receiver and medium access control (MAC) showing modulated data input from a transmission medium, such as a coaxial cable, to the upstream burst receiver and showing digital data output from the MAC;

FIG. 5 is a block diagram showing an aspect of the present invention wherein a spectrum management/allocation circuit monitors at least one channel characteristic such as signal-to-noise ratio (SNR) or channel power and/or the spectrum management/allocation circuit monitors channel statistics such as packet/forward error correction (FEC) status and the spectrum management/allocation circuit subsequently defines the upstream channel frequency or spectral allocation based thereupon;

FIG. 6 is a chart showing RS coding gain for various T's using 16-QAM with K equals 64 bytes;

FIG. 7 is a schematic drawing providing an example of fine frequency agility;

FIG. 7A is a schematic representation of a data packet showing the positioning of the data or payload therein and also showing the location of a guard band;

FIG. 8 is a flowchart showing dynamic channel allocation control flow;

FIG. 9 is a graphical representation of the relationship of the minislots which define the request interval, maintenance interval and data interval with respect to the minislot clock (MSCLK);

FIG. 10 is a graphical representation of the MAP message format prior to message filtering;

FIG. 11 is a graphical representation of the MAP message format after message filtering;

FIG. 12 is a block diagram showing the architecture of the shared SRAM-based MAP interface for eight upstream channels;

FIG. 13 is a block diagram showing the MAP timing control interface signals which are transmitted from the MAP to the demodulator of the burst receiver;

FIG. 14 is a graphical representation of the relationship between the minislots which define the request interval, the maintenance interval and the data interval with respect to the minislot clock, MapValid signal and MapData and also showing the MAP clock;

FIG. 15 is a graphical representation of the relationship between the minislots which define the maintenance interval, the minislot clock, the MapValid signal and MapData and also showing the timing of the receive now (Rx_now) signal;

FIG. 16 is a graphical representation of the relationship between the minislots which define the data interval, the minislot clock, the MapValid signal and MapData and also showing the timing of the receive now (Rx_now) signal;

FIG. 17 is a graphical representation of the relationship between the minislots which define the request interval, the minislot clock, the MapValid signal and MapData and also showing the timing of the receive now (Rx_now) signals;

FIG. 18 is a graphical representation showing the prepend information when the first block TDMA transmission bit is set;

FIG. 19 is a graphical representation showing the prepend information when the equalizer prepend bit is set, thereby increasing the prepend information by 32 bits (for a total length of 48 bits) with respect to FIG. 18;

FIG. 20 is a table showing the statistics and the calculation used for each slot definition;

FIG. 21 is a block diagram of the MAC/PHY interface;

FIG. 22 is a graphical representation showing the relationship of the bit clock with respect to the burst valid indicator (BlkDV) and the data;

FIG. 23 is a graphical representation showing the format of the prepend data;

FIG. 24 (should follow FIG. 22) shows the signaling for the data/control interface termination system from ;

FIG. 25 is a block diagram showing the sign-on sequence for the cable modem initialization process;

FIG. 26 is a block diagram showing the relationship of the cable modem to the cable modem termination system;

FIG. 27 is a graphical representation showing the MAP serial interface field definitions;

FIG. 28 is a graphical representation showing the contents of the prepended information;

FIG. 29 is a table showing the definitions of the bit fields for the status bytes in the prepended information;

FIG. 30 is a block diagram showing the burst demodulator status processing flow;

FIG. 31 is a block diagram showing the burst detector SPI bus interface;

FIG. 32 is a timing diagram showing the generic byte base serial input with control information prepended and TXSP=1; and

FIG. 33 is a timing chart showing the generic byte base serial input interface with control information prepended and TXSP=0.

Method and Apparatus for Reducing Noise in a Bidirectional Cable Transmission System

FIG. 1 is a schematic block diagram of a bidirectional cable transmission system;

FIG. 2 is a schematic block diagram of a portion of the RF receiver at the headend of the cable system shown in FIG. 1;

FIG. 3 is a schematic block diagram of the adaptive notch filter shown in FIG. 2;

FIG. 4 is a schematic block diagram of the generalized decision feedback equalizer (DFE) shown in FIG. 2;

FIG. 5 is a schematic block diagram of a portion of one of the cable modems shown in FIG. 1;

FIG. 6 is a diagram of the TDMA slots for transmitting information in an upstream channel of the cable system shown in FIG. 1;

FIG. 7 is a block diagram of a method for reducing noise in the cable system shown in FIG. 1;

FIGS. 8A-8C are frequency response diagrams illustrating common noise (such as ingress) cancellation according to the method shown in FIG. 7;

FIGS. 9A and 9B are diagrams of a 16-QAM constellation before and after noise cancellation according to the method shown FIG. 7; and

FIGS. 10A, 10B, and 10C are frequency response diagrams illustrating both ingress and individual noise compensation according to the method shown in FIG. 7.

DETAILED DESCRIPTION OF THE INVENTION

In a cable modem system, a headend or cable modem termination system (CMTS) is located at cable company facility and functions as a modem which services a large number subscribers. Each subscriber has a cable modem (CM). Thus, the cable modem termination system must be capable of facilitating bidirectional communication with any desired one of the plurality of cable modems.

As used herein, the cable modem termination system (CMTS) is defined to include that portion of a headend which facilitates communication with a plurality of cable modems. A typical cable modem termination system includes a burst receiver, a continuous transmitter and a medium access control (MAC).

The cable modem termination system communicates with the plurality of cable modems via a hybrid fiber coaxial (HFC) network, wherein optical fiber provides communication to a plurality of fiber nodes and each fiber node typically serves approximately 500 to 2,000 subscribers, which communicate with the node via coaxial cable. A plurality of subscribers communicate with the fiber node via a common or shared coaxial cable. It is this sharing of the common coaxial cable which necessitates that the number of cable modems attached thereto be limited so as to mitigate the likelihood of undesirable bit rate reductions which inherently occur when an excessive number of cable modems communicate simultaneously over a single coaxial cable.

The hybrid fiber coaxial network of a cable modem system utilizes a point-to-multipoint topology to facilitate communication between the cable modem termination system and the plurality of cable modems. Frequency domain multiple access (FDMA)/time division multiplexing (TDM) is used to facilitate communication from the cable modem termination system to each of the cable modems, i.e., in the downstream direction. Frequency domain multiple access (FDMA)/time domain multiple access (TDMA) is used to facilitate communication from each cable modem to the cable modem termination system, i.e.,in the upstream direction.

The cable modem termination system includes a downstream modulator for facilitating the transmission of data communications therefrom to the cable modems and an upstream demodulator for facilitating the reception of data communications from the cable modems.

The downstream modulator of the cable modem termination system utilizes either 64 QAM or 256 QAM in a frequency band of 54 MHz to 860 MHz to provide a data rate of up to 56 Mbps.

Since the upstream channel has a much lower data rate requirement, the upstream demodulator uses either QPSK or 16 QAM in a frequency range of 5 MHz to 42 MHz to provide a data rate of up to 10 Mbps.

The asymmetric data throughput defined by the upstream channel requiring a much lower data rate than the downstream channel results from the inherently larger amount of data which is communicated via the downstream channel during pay-per-view, Internet access and the like, wherein a video signal is communicated via the downstream channel, while only control signals such as those associated with viewing of the video signal are communicated via the upstream

channel. Thus, the downstream channel requirement may exceed 1.5 Mbps, while the upstream channel requirement may be as low as 16 Kbps.

Similarly, each cable modem includes an upstream modulator for facilitating the transmission of data to the cable modem termination system and a downstream demodulator for receiving data from the cable modem termination system. The upstream modulator of each cable modem uses either QPSK or 16 QAM within the 5 MHz to 42 MHz bandwidth of the upstream demodulator and the downstream demodulator of each cable modem utilizes either 64 QAM or 256 QAM in the 54 MHz to 860 MHz bandwidth of the downstream modulator (in North America).

Contemporary cable modem systems operate on a plurality of upstream channels and utilize time division multiple access (TDMA) in order to facilitate communication between a plurality of cable modems and a single cable modem termination system on each upstream channel. Typically, between 250 and 500 cable modems communicate with a single cable modem termination system on a given upstream channel.

In order to accomplish TDMA for upstream communication, it is necessary to assign time slots within which cable modems having a message to send to the cable modem termination system are allowed to transmit. The assignment of such time slots is accomplished by providing a request contention area in the upstream data path within which the cable modems are permitted to contend in order to place a message which requests additional time in the upstream data path for the transmission of their message. The cable modem termination system responds to these requests by assigning time slots to the cable modems making such a request, so that as many of the cable modems as possible may transmit their messages to the cable modem termination system utilizing TDMA and so that the transmissions are performed without undesirable collisions.

Because of the use of TDMA, the cable modem termination system must use a burst receiver, rather than a continuous receiver, to receive data packets from cable modems via upstream communications. As those skilled in the art will appreciate, a continuous receiver can only be utilized where generally continuous communications (as opposed to burst communications as in the present invention) are performed, so as to substantially maintain timing synchronization between the transmitter and the receiver, as is necessary for proper reception of the communicated information. During continuous communications, timing recovery is a more straightforward process since signal acquisition generally only occurs at the initiation of such communications. Thus, acquisition is generally only performed in continuous receivers once per continuous transmission and each continuous transmission may be very long.

However, the burst communications inherent to TDMA systems require periodic and frequent reacquisition of the signal. That is, during TDMA communications, the signal must be reacquired for each separate burst transmission being received.

Since continuous receivers generally only acquire the signal once, the need to minimize acquisition time is much less critical in continuous receivers than in burst receivers, wherein acquisition must be performed for each separate burst, and therefore occurs quite frequently. Thus, there is a strong motivation to minimize acquisition time in burst receivers, so as to

enhance overall data transmission efficiency and throughput. As such, it is beneficial to provide techniques which enhance the speed at which data packets transmitted according to TDMA methodologies may be acquired by a burst receiver, such as that of a cable modem termination system.

Data Packet Fragmentation in a Cable Modem System

In accordance with the present invention, data packets are transmitted from the cable modems to the cable modem termination system within time slots which are allocated by the cable modem termination system and wherein a data packet is fragmented or divided among a plurality of time slots when a time slot which is sufficiently large to contain the data packet cannot be defined due to data flow and bandwidth constraints.

The assignment of such time slots is accomplished by providing a request contention area in the upstream data path within which the cable modems are permitted to contend in order to place a message which requests additional time in the upstream data path for the transmission of their message. The cable modem termination system responds to these requests by assigning time slots to the cable modems making such a request, so that as many of the cable modems as possible may transmit their messages to the cable modem termination system utilizing TDMA and so that the transmissions are performed without undesirable collisions. This time slot assignment by the cable modem termination system is known as a grant because the cable modem termination system is granting a particular cable modem permission to use a specific period of time in the upstream.

The cable modem termination system usually tries to match the grant to the request so that the cable modem is given sufficient bandwidth for its transmission.

It is not always possible for the cable modem termination system to allocate a sufficiently large time slot in response to a request from the cable modem so as to contain all of the data packet for which the request was sent. This insufficiently large time slot allocation is referred to as a partial grant. This may happen, for example, when upstream traffic between the cable modems and the cable modem termination system is heavy. Thus, in such instances, it is desirable to divide or fragment the data packet among a plurality of such time slots. Another example is when the cable modem termination system supports constant bit rate services, such as voice, in the upstream direction. These services require grants at periodic intervals. When supporting these types of services, the cable modem termination system may need to send a partial grant to one modem in order to schedule a constant bit rate service for another modem.

It is desirable to define a system for fragmenting data packets which minimizes wasted bandwidth. In accordance with the present invention, a technique is provided for fragmenting data packets in a cable modem system wherein data packets larger than an allocated time slot are split among a plurality of time slots.

In response to receiving the request, the cable modem termination system allocates a time slot for transmission of at least a portion of the data packet from the cable modem to the cable modem termination system. Alternatively, the allocation may be performed by a different device,

e.g., a device other than the cable modem termination system, referred to herein generally as a dynamic time slot controller.

Information representative of the time slot is transmitted from a dynamic time slot controller, such as the cable modem termination system, to the cable modem.

At least a portion of the data packet is transmitted from the cable modem to the cable modem termination system within the allocated time slot. Transmitting at least a portion of the data packet from the cable modem to the cable modem termination system within the time slot mitigates undesirable collisions between data packets which are transmitted by different cable modems to the cable modem termination system upon a common frequency channel. Thus, the simultaneous transmission of data packets by different cable modems upon a common frequency channel is prevented.

When the time slot allocated for the transmission of the data packet from the cable modem to the cable modem termination system is sufficient for transmission of only a portion of the data packet for which the request was transmitted, then the cable modem transmits only a portion of the data packet for which the request was transmitted and the cable modem termination system allocates at least one additional time slot and transmits to the cable modem information representative of the additional time slot(s), so as to facilitate transmission of the remaining portion of the data packet from the cable modem to the cable modem transmission system.

Occasionally, due to bandwidth constraints and the amount of data flow on a given channel, it is not possible to allocate a time slot which is sufficient for transmission of the entire data packet for which a request was received by the cable modem termination system. Rather than denying the request altogether, according to the present invention, a time slot is allocated by the dynamic time slot controller so as to facilitate the transmission of at least a portion of the data packet from the cable modem to the cable modem termination system. One or more additional time slots are then allocated to facilitate transmission of the remaining portion of the data packet from the cable modem to the cable modem termination system. Thus, the remaining portion of the packet may be split or fragmented among a plurality of such additional time slots, if necessary.

Briefly, upstream data transmission on an upstream channel is initiated by a request made by a cable modem for a quantity of bandwidth, i.e., a plurality of time slots, to transmit data comprising a message. The size of the request includes payload, i.e., the data being transmitted, and overhead, such as preamble, FEC bits, guard band, etc. After the request is received at the headend, the CMTS grants bandwidth to the requesting cable modem and transmits the size of the grant and the specific time slots to which the data is assigned for insertion to the requesting cable modem. If the grant is smaller than the size of the request, i.e., a partial grant, the cable modem senses this condition and separates data into two or more fragments for transmission. : If the cable modem has not received an additional grant or grant pending prior to the transmission time of the partial grant, the cable modem inserts a request for additional bandwidth into the fragment header. This bandwidth request, called a piggyback request, is for the amount of bandwidth required to send the remainder of the packet. If the cable modem has received an additional grant or grant pending prior to the transmission time of the partial grant, the cable

modem assigns a value of zero to the piggyback request field in the fragment header. The cable modem transmits the first fragment in the assigned time slots. The cable modem treats each subsequent grant in the same manner. If additional grants (or grant pendings) are enqueued at the cable modem during the transmission time of a fragment, the cable modem does not include a piggyback request. If additional grants are not enqueued at the cable modem during the transmission time of a packet or fragment, the cable modem inserts a piggyback request for enough bandwidth to transmit the remainder of the packet being fragmented. The piggyback field of the last fragment of a packet can be used to transmit a request for the amount of bandwidth necessary to transmit the next packet enqueued at the cable modem.

The CMTS can operate in either of two different modes: multiple grant mode or piggyback mode. In multiple grant mode, the CMTS must retain the state of fragmentation for each modem.

The CMTS allots bandwidth to the requesting cable modem and determines the amount of data required to fill the allotted bandwidth, taking into account the overhead required to transmit the fragment, and sends a partial grant for the fragmented data to the cable modem. The CMTS also transmits to the cable modem a partial grant for the remaining data fragment if there is bandwidth available in the current MAP or a grant pending if bandwidth must be provided by a subsequent MAP. A grant pending signal is sent in each subsequent MAP until the grant can be fulfilled. In this mode, the cable modems insert fragmented data pursuant to the grants as determined by the CMTS.

In multiple grant mode, the CMTS does not need to retain the state of fragmentation for each modem. The CMTS allots bandwidth to the requesting cable modem and the requesting cable modem

determines the amount of data required to fill the allotted bandwidth, taking into account the overhead required to transmit the fragment. The requesting cable modem inserts such data in the assigned time slots and checks for partial grants or pending grants from the CMTS. If there are none, this is a signal to the cable modem that the piggyback mode should be used. The requesting cable modem inserts a request for the remainder of the data, including the amount of remaining data, in a piggyback field of the fragment header transmitted to the CMTS. (In the multiple request mode, the piggyback field that accompanies a transmitted data fragment is set to zero.) Responsive to the request in the piggyback field the CMTS transmits another grant to transmit data to the requesting cable modem. If the alloted time slots are insufficient to transmit the entire data fragment, the process is repeated until all the data has been transmitted. In the piggyback mode, the cable modem retains the state of fragmentation, i.e., it keeps track of the remainder of the data to be transmitted during the fragmentation process.

In summary, the cable modem is capable of operating either in the multiple grant mode or the piggyback mode, depending on how the CMTS allocates grants. If the CMTS generates partial grants or pending grants, this is sensed by the cable modem and the cable modem operates in the multiple grant mode. If the CMTS does not generate partial grants or pending grants, this is sensed by the cable modem and the cable modem operates in the piggyback mode.

The size of the payload that can be transmitted in a specified number of time slots depends on the burden imposed by the data transmission format. This size is called the burdened PHY length. In one embodiment, the burdened PHY length is determined by a forward lookup table using the total length of the data in bytes as an index. Each time a request is made by a cable modem, the forward lookup table is accessed using the total length and the burdened PHY length is retrieved for transmission to the CMTS as the request. Grants are transmitted to the cable modems in terms of burdened PHY length. The total length of the data in bytes that can be transmitted pursuant to a grant is determined by a reverse lookup table using the burdened PHY length as an index. The forward and reverse lookup tables are created each time that the burst profile changes and are stored in memory for use in processing requests and grants at the cable modem. Alternatively, the conversion between total length and burdened PHY length could be carried out as described in application No. 60/115,998 filed on January 15, 1998.

The operation of the cable modem in transmitting fragmented data is illustrated by the following example considered with FIG. 19.

1. (Requesting State) - CM wants to transmit a 1018 byte packet. CM calculates how much physical layer overhead (POH) is required and requests the appropriate number of minislots. CM makes a request in a contention region. Go to step 2.

2. (Waiting for Grant) - CM monitors MAPs for a grant or grant pending for this SID. If the CM's ACK time expires before the CM receives a grant or grant pending, the CM retries requesting for the packet until the retry count is exhausted - then the CM gives up on that packet. Go to step 3.

3. (First Fragment) - Prior to giving up in step 2, the CM sees a grant for this SID that is less than the requested number of minislots. The CM calculates how much MAC information can be sent in the granted number of minislots using the specified burst profile. In the example in Figure 19, the first grant can hold 900 bytes after subtracting the POH. Since the fragment overhead (FRAG HDR, FHCS, and FCRC) is 16 bytes, 884 bytes of the original packet can be carried in the fragment. The CM creates a fragment composed of the FRAG HDR, FHCS, 884 bytes of the original packet, and an FCRC. The CM marks the fragment as first and prepares to send the fragment. Go to step 4.

4. (First Fragment, multiple grant mode) - CM looks to see if there are any other grants of grant pendings enqueued for this SID. If so, the CM sends the fragment with the piggyback field in the FRAG HDR set to zero and awaits the time of the subsequent grant to roll around. - - to step 6. If there are not any grants or grant pendings, go to step 5.

5. (First Fragment, piggyback mode) - If there are no other grants or grant pendings for this SID in this MAP, the CM calculates how many minislots are required to send the remainder of the fragmental packet, including the fragmentation overhead, and physical

layer overhead, and inserts this amount into the piggyback field of the FRAG HDR. The CM then sends the fragment and starts its ACK timer for the piggyback request. In the example in Figure 19, the CM sends up a request for enough minislots to hold the POH plus 150 bytes (1018-884+16). Go to step 6.

6. (Waiting for Grant). The CM is now waiting for a grant for the next fragment. If the CM's ACK timer expires while waiting on this grant, the CM should send up a request for enough minislots to send the remainder of the fragmented packet, including the fragmentation overhead, and physical layer overhead. Go to step 7.

7. (Receives next fragment grant) - Prior to giving up in step 6, the CM sees another grant for this SID. The CM checks to see if the grant size is large enough to hold the remainder of the fragmented packet, including the fragmentation overhead and physical layer overhead. If so, go to step 10. If not, go to step 8.

8. (Middle Fragment, multiple grant mode) - Since the remainder of the packet (plus overhead) will not fit in the grant, the CM calculates what portion will fit. The CM encapsulates this portion of the packet as a middle fragment. The CM then looks for any other grants or grant pendings enqueued for this SID. If either are present, the CM sends the fragment with the piggyback field in the FRAG HDR set to zero and awaits the time of the subsequent grant to roll around. - - go to step 6. If there are not any grants or grant pendings, go to step 9.

9. (Middle Fragment, piggyback mode). The CM calculates how many minislots are required to send the remainder of the fragmented packet, including the fragmentation overhead and physical layer overhead, and inserts this amount into the piggyback field of the FRAG HDR. The CM then sends the fragment and starts its ACK timer for the piggyback request. Go to step 6.

The described fragmentation capability can be enabled or disabled in the cable modems on a selective basis. Specifically, when a cable modem transmits a registration message to the CMTS at the time that the cable modem enters service, the acknowledging response of the CMTS includes a signal that either enables or disables fragmentation. If fragmentation is enabled, the cable modem and the CMTS operate as described above to fragment data to be transmitted upstream. If fragmentation is disabled, the cable modem only transmits data to the headend if the granted amount of bandwidth is the same as or larger than the bandwidth required to transmit the data. Alternatively, if fragmentation is disabled, the CMTS only transmits a grant if the requested bandwidth is the same as or smaller than the bandwidth available for transmission to the headend.

It is important to understand that a plurality of such cable modems are present in a cable modem system and that each of the cable modems may, periodically, transmit a request for a time

slot allocation to the cable modem termination system. Thus, the cable modem termination system frequently receives such requests and allocates time slots in response to such requests. Information representative of the allocated time slots is compiled to define a MAP and the MAP is then broadcast to all of the cable modems on a particular channel, so as to provide information to all of the cable modems which have one or more data packets to transmit to the cable modem termination system precisely when each of the cable modems is authorized to transmit its data packet(s). Thus, the present invention facilitates the coordinated transmission of data packets from each of the cable modems to the cable modem termination system according to time division multiple access (TDMA).

The allocation of time slots, by the cable modem termination system, for example, and the generation of a MAP which defines the time slot allocations is described in detail below.

Referring now to FIG. 1, the fragmentation of a data packet by a cable modem into first and second portions thereof is shown, wherein the first portion of the data packet is placed in a first time slot allocated by the cable modem termination system and the second portion of the data packet is placed in a second time slot allocated by the cable modem termination system.

As shown in FIG. 1, a data packet 10 which is too large to fit within a first time slot 117a is fragmented by an appropriate device such as a cable modem such that a first portion 10a of the data packet 10 is placed in the first time slot 117a and the remaining or second portion 10b of the data packet 10 is placed within the second time slot 117b of the upstream channel 117.

For example, if the maximum size of each time slot 117a, 117b is 256 symbols and the data packet 10 conforms 300 symbols, then 256 symbols of the data packet 10 are put into the first time slot 117a and the remaining 44 symbols are put into the second time slot 1176.

This placing of the data packet 10, whether fragmented or not, within the allocated time slots 117a and 117b prevents undesirable collisions among a plurality of such data packets transmitted by a corresponding plurality of cable modems upon a given frequency channel. The use of guard bands 9 in the upstream channel 117 tend to further mitigate the occurrence of such undesirable collisions by providing an unused time space between each time slot of the upstream channel 117 so as to accommodate differences in synchronization between the cable modem termination system and the various cable modems.

Referring now to FIG. 2, a hybrid fiber coaxial (HFC) network 44 facilitates the transmission of data between a headend 12, which includes at least one cable modem termination system, and a plurality of homes 14, each of which contains a cable modem. Such hybrid fiber coaxial networks are commonly utilized by cable providers to provide Internet access, cable television, pay-per-view and the like to subscribers and download data include Internet related data, TV programs and the like downstream to the user.

In the example shown in the figure, approximately 500 homes 14 are in electrical communication with each node 16, 34 of the hybrid fiber coaxial network 44, typically via coaxial cable 29, 30, 31. Amplifiers 15 facilitate the electrical connection of the more distant homes 14 to the nodes 16, 34 by boosting the electrical signals so as to desirably enhance the signal-to-noise ratio of such communications and then transmitting the electrical signals over

coaxial conductors 30, 31. Coaxial conductors 29 electrically interconnect the homes 14 with the coaxial conductors 30, 31, which extend between amplifiers 15 and nodes 16.

Each node 16, 34 is electrically connected to a hub 22, 24, typically via an optical fiber 28. The hubs 22, 24 are in communication with the headend 12, via optical fiber 20, 26. Each hub is typically capable of facilitating communication with approximately 20,000 homes 14.

The optical fiber 20, 26 extending intermediate the headend 12 and each hub 22, 24 defines a fiber ring which is typically capable of facilitating communication between approximately 100,000 homes 14 and the headend 12.

The headend 12 may include video servers, satellite receivers, video modulators, telephone switches and/or Internet routers 18, as well as the cable modem termination system.

Referring now to FIG. 3, a simplified block diagram shows the interconnection of the headend 12 and an exemplary home 14, wherein a cable modem 190 communicates with a cable modem termination system, embodied as a line card 42, via hybrid fiber coaxial network 44.

More particularly, a personal computer 48, disposed within the home 14, is connected via cable 10 to the cable modem 190 which communicates via coaxial cable link 29, which may be a physical cable, radio frequency (RF) or other data transfer link with the hybrid fiber coaxial network 44, which in turn communicates via optical fiber 20 with the line card or cable modem termination system (CMTS) 42 of the headend 12. Internet router 40 facilitates communication between the headend 12 and the Internet.

Referring now to FIG. 4, the contents of a MAP protocol data unit (PDU) 113 are shown. The MAP PDU 113, which is transmitted on the downstream channel by the cable modem termination system 42 (FIG. 3) to all of the cable modems 190 on a given frequency channel, contains the time slot allocations for at least some of the cable modems 190 which have previously sent a request to transmit one or more data packets to the cable modem termination system 42. When the channel bandwidth is sufficient, in light of the number of such requests received by the cable modem termination system 42, then the cable modem termination system 42 allocates a time slot for each such requesting cable modem 190.

Further, the MAP PDU 113 at least occasionally defines at least one request contention region 112 and generally also contains a plurality of cable modem transmit opportunities 114 within the upstream channel 117. A maintenance frame 116 may also be defined by the MAP PDU 113 within the upstream channel 117, as discussed in detail below.

The request contention region 112 includes at least one time area within which the cable modems 190 transmit their requests to transmit data packets to the cable modem termination system 42. Each of the cable modem transmit opportunities 114 define a time slot within which a designated cable modem 190 is permitted to transmit the data packet for which the request was previously sent to the cable modem termination system 42.

Additionally, one or more optional transmit contention regions (not shown) may be provided wherein cable modems 190 may contend for the opportunity to transmit data therein. Such transmit contention regions are provided when sufficient bandwidth is left over after the MAP PDU 113 has allocated transmit opportunities 114 to all of those cable modems 190 which

have requested a time slot allocation. Thus, transmit contention regions are generally provided when upstream data flow is comparatively light.

The upstream channel 119, is divided into a plurality of time intervals 110, each of which may optionally be further subdivided into a plurality of sub-intervals 115. The upstream channel 119 thus partitioned so as to facilitate the definition of time slots, such that each of a plurality of cable modems 190 may transmit data packets to the cable modem termination system 42 without interfering with one another, e.g., without having data collisions due to data packets being transmitted at the same time.

Thus, the use of a MAP 113 facilitates the definition of slots 92. Each slot 92 may be used for any desired predetermined purpose, e.g., as a request contention region 112 or a transmit opportunity 114. Each slot 92, as defined by a MAP PDU 113, includes a plurality of time intervals 110 and may additionally comprise one or more sub-intervals 115 in addition to the interval(s) 110. The number of intervals 110 and sub-intervals 115 contained within a slot 92 depends upon the contents of the MAP PDU 113 which defines the slot 92. The duration of each interval 110 and sub-interval 115 may be defined as desired. Optionally, each sub-interval 115 is approximately equal to a media access control (MAC) timing interval. Each MAP PDU 113 defines a frame and each frame defines a plurality of slots 92.

The beginning of each sub-interval 115 is aligned in time with the beginning of each interval 110 and each interval 110 typically contains an integral number of sub-intervals 115.

Typically, the request contention region 112 and each cable modem transmit opportunity 114 includes a plurality of integral time intervals 110. However, the request contention region 112 and/or the cable modem transmit opportunity 114 may alternatively include any desired combination of intervals 110 and sub-intervals 115.

Thus, according to the present invention, each request contention region 112 may be utilized by a plurality of the cable modems 190 to request one or more time slot allocations which facilitate the transmission of one or more data packets during the cable modem's 190 subsequently allocated transmit opportunity 114.

Each data packet may contain only data, although an extended data packet may be defined to include both data and a preamble. The preamble is typically stripped from an extended packet by the cable modem termination system 42 and the data in the packet is then processed by a central processing unit of the cable modem termination system 42.

The duration of the request contention region 112 is typically variable, such that it may be sized to accommodate the number of cable modems 190 expected to request time slot allocations from the cable modem termination system 42. The duration of the request contention region 112 may thus be determined by the number of requests transmitted by cable modems as based upon prior experience.

The time slot allocations 92 defined by cable modem transmit opportunities 114 may optionally be defined, at least in part, on the basis of priorities established by the cable modem termination system 42 for different cable modems 190. For example, priorities may be established for individual cable modems 190 on the basis of an election made by the subscribers,

which is typically dependent upon the type of service desired. Thus, a subscriber may elect to have either a premium (high priority) service or a regular (low priority) service.

Alternatively, priorities may be established by the cable modem termination system 42 for the cable modems based upon size and number of cable modem transmit opportunities 114 historically requested by the subscribers. Thus, a cable modem that typically requires a large number of time intervals 110 may be defined as a high priority user, and thus given priority in the allocation of time slots within a cable modem transmit opportunity 114, based upon the assumption that such large usage is indicative of a continuing need for such priority, e.g., is indicative that the subscriber is utilizing cable television, pay-per-view or the like.

Alternatively, the cable modem termination system may assign such priorities based upon the type of service being provided to each cable modem. Thus, for example, when cable television or pay-per-view is being provided to a cable modem, then the priority of that cable modem may be increased, so as to assure uninterrupted viewing.

The priority associated with each cable modem 190 may determine both the size of time slots allocated thereto and the order in which such allocations are performed. Those allocations performed earlier in the allocation process are more likely to be completely filled than those allocations performed later in the allocation process. Indeed, allocations performed later in the allocation process may go unfilled, when the bandwidth of the channel is not sufficient to facilitate allocation of time slots for all requesting cable modems 190.

Time slots which define the maintenance region 116 are optionally provided in a MAP 113. Such maintenance regions 116 may be utilized, for example, to facilitate the synchronization of the clocks of the cable modems with the clock of the cable modem termination system. Such synchronization is necessary in order to assure that each cable modem 190 transmits only within its allocated time slots, as defined by each cable modem's transmit opportunity 114.

The request contention region 112 cable modem transmit opportunity 114 and maintenance region 116 typically begin at the beginning of an interval 110 and end at the end of an interval 110. However, each request contention region 112, cable modem transmit opportunity 114 and maintenance region 116, may begin and end anywhere as desired.

Thus, according to the present invention, variable duration request contention regions 112, cable modem transmit opportunities 114 and maintenance regions 116 are provided. Such variable duration request contention regions 112, transmit opportunities 114 and maintenance regions 116 facilitate flexible operation of the cable modem system and enhance the efficiency of data communications on the cable modem system by tending to mitigate wasted channel capacity.

The current MAP 170 is transmitted in the downstream channel 111 after transmission of a previous MAP 90 and before any subsequent MAPs 91. Data, such as data packets associated with web pages, e-mail, cable television, pay-per-view television, digital telephony, etc. are transmitted between adjacent MAPs 90, 170, 91.

The contents of each cable modem transmit opportunity 114 optionally include data and a preamble. The data includes at least a portion of the data packet for which a request to transmit

was sent to the cable modem termination system 42. The preamble typically contains information representative of the identification of the cable modem 190 from which the data was transmitted, as well as any other desired information.

The data and the preamble do not have to occupy the full time interval of the cable transmit opportunity 114. Guard bands 9 (FIG. 1) are optionally provided at the beginning and end of each slot, so as to decrease the precision with which time synchronization between the cable modem termination system and each cable modem must be performed. Thus, by providing such guard bands, some leeway is provided in the transmit time during which each cable modem inserts its data packet into the upstream channel 119.

Referring now to FIG. 5, the interrelationship of the MAC frames 118 of the MAC layer and the frames 128, each of which contain at least one, generally a plurality, of data 122 and forward error correction (FEC) 124 portions which, taken together, occupy an allocated time slot 92 (FIG. 4) which defines a request contention region 112.

Each MAC frame 118 further includes, at the physical layer, PHY overhead portion 120. The PHY overhead 120 contains physical layer overhead information.

Additional PHY overhead 126 generally follows the forward error correction (FEC) 124 portion and optionally includes a guard band 9 (FIG. 1) which reduces the accuracy with which synchronization of the cable modems must be performed. That is, the guard band of the physical overhead 126 provides a tolerance, such that the cable modems 190 do not have to transmit precisely within their allocated time slots 92.

Each MAC frame 118 includes at least one PHY overhead 120, one data portion 122 and forward error correcting (FEC) 124. Optionally, each MAC frame 118 may include a plurality of data portions 122 and corresponding forward error correcting (FEC) portions 124, if desired.

Referring now to FIG. 6, a block diagram shows how the cable modem termination system 42 headend 12 processes the priorities of requests made by the cable modems 190 to send data to the cable modem termination system 42. As indicated by block 130, the cable modem termination system 42 sends an initial or current MAP 170 (FIG. 4) based upon data previously collected from the cable modems 190 during the sending of a MAP 90 previous to the initial MAP 170. At the same time, the cable modem termination system 42 sets the time for the MAP 91 subsequent to the initial or current MAP 170. The time for the subsequent MAP 91 is based upon the time for the sending of the initial MAP 170 and is set for a time after the sending of the initial MAP.

As indicated by block 132, the cable modem termination system 42 collects collision statistics for the next MAP 91 while the initial or current MAP 170 is being processed. These statistics indicate collisions in time between bursts from different cable modems 190. When the current time becomes greater than the next MAP time, as indicated in block 131, then the MAP building process begins as indicated in block 133.

When an upstream request arrives, block 135, then the requests for sending data in the next MAP 91 are then processed to determine if the requests are high priority bandwidth requests block 136 or low priority bandwidth requests block 137. If the request is a high priority bandwidth request, the request is placed in a high priority bandwidth request queue as indicated

at block 138. If the request is a low priority bandwidth request, the request is placed in a low priority bandwidth request queue as indicated at block 139.

When a request is placed in either a high priority bandwidth request queue 138 or a low priority bandwidth request queue 139, a portion of the MAC, depicted as a line 140, provides a sequence for collecting collision statistics for the next MAP 91. Such a sequence is also provided when a request is processed and is found to be neither a high priority bandwidth request 136 nor a low priority bandwidth request 137.

Referring now to FIGs. 7 and 8, the construction of a frame is shown. As shown in block 143, requests are made by the cable modems 190 in a request contention region 112 (FIG. 4) of a first MAP for the grant or allocation by the cable modem termination system 42 to the subscribers of Information Elements (IE). An Information Element may be considered to be the same as a region. A maintenance opportunity is optionally provided as shown at block 144. Such maintenance opportunities may, for example, be used to synchronize the operation of the cable modem 190 with the operation of the cable modem termination system 42. As previously indicated, this maintenance opportunity may be provided only periodically.

A determination is then made at block 146 as to whether the high priority request queue is empty. If the answer is No with respect to the high priority request queue, a determination is then made at block 148 as to whether the frame length is less than a desired length. If the answer is Yes, the request of the subscriber to transmit data is granted and the frame length is incremented by the size of the data requested at block 150.

If the high priority request queue is empty, a determination is made at block 152 as to whether the low priority request queue is empty. If the answer is No, a determination is made at block 154 as to whether the frame length will be less than the desired length. If the answer is Yes with respect to the low priority request queue, the request of the cable modem 190 to transmit data to the cable modem termination system 42 is granted and the frame length is incremented by the size of the grant. This is indicated at block 156.

It may sometimes happen that the frame length will be at least equal to the desired length when the request with respect to the high priority request queue is introduced to the block 148. Under such circumstances, the request is not granted and a determination is then made as to whether the low priority request queue is empty. Similarly, if the frame length will be greater than the desired frame length when a request with respect to the low priority request queue is made, the request is not granted. An indication is accordingly provided on a line 157 when the high priority request queue and the low priority request queue are both empty or when the frame length will be at least as great as the desired length.

When the high priority request queue and the low priority request queue are both empty or when the frame length will be at least as great as the desired length upon the assumed grant of a request, a determination is made, as at block 158 (FIG. 8) as to whether the request queues are empty. This constitutes an additional check to make sure that the queues are empty. If the answer to such determination is No, this indicates that the frame length will be greater than the desired frame length upon the assumed grant of a request. Under such circumstances, a grant of a zero length is provided in the MAP 170 for each request in each queue. This zero length grant

is provided so that the headend can notify the subscriber that the request has not been granted but was received by the headend. In effect, a zero length grant constitutes a deferral. The request was seen, i.e., not collided, but not granted yet. It will be granted in a subsequent MAP 91.

If a determination is made as at block 158 that the request queues are empty, a determination is then made at block 162 as to whether the frame length will be less than the desired frame length. If the answer is Yes, the frame is padded to the desired length with data from a contention data region 168 (FIGs. 9 and 10) in the frame, as indicated at block 164. The contention data region 168 constitutes an area of reduced priority in the frame. It provides for the transmission of data from the cable modems 190 to the cable modem termination system 42 via available slots in the frame where cable modems have not been previously assigned slots by the cable modem termination system 42. The contention data region does not require a grant by the cable modem termination system 42 of a request from a cable modem 190 as in the request contention data region 112 in FIG. 4. Since no grant from the cable modem termination system 42 is required, the contention data region 168 in FIGs. 9, 10 provides faster access to data for the subscriber than the request contention region 112. The contention data region 168 is described below in additional detail in connection with the showing of FIGs. 9 and 10.

Available slots in a frame are those that have not been assigned on the basis of requests from the cable modems 190. As indicated at block 166 in FIG. 8, the cable modem termination system 42 acknowledges to the cable modem 190 that the cable modem termination system 42 has received data from the contention data region (FIGs. 9 and 10) in the frame. The cable modem termination system 42 provides this acknowledgment because the cable modem 190 would not otherwise know that such data was not involved in a data collision and has, indeed, has been received from the contention data region 168.

Referring now to FIGs. 9 and 10, a block diagram of that portion of the cable modem termination system 42 which receives requests from the cable modems 190 and which generator MAPs in response to those requests is shown.

The contention data region 168 in FIG. 10 is included in frame 118 defined by a MAP 111 (FIG. 4). The frame 118 in FIG. 9 may include a number of other regions. One region is indicated at 172 and is designated as contention requests region 112 in FIG. 4. It includes slots designated as X 181. In these slots X 181, collisions between request data from different cable modems 190 have occurred. Other slots in the contention request region 172 are designated as R 183. Valid uncollided request data is present in these slots. The contention request region 172 also illustratively includes an empty slot 175. None of the subscribers 14 has made a request in this empty slot 175.

A cable modem transmit opportunity region 176 (corresponding to the cable modem transmit opportunity region 114 in FIG. 4) may also be provided in the frame 118 adjacent the contention request area 172. As previously indicated, individual cable modems 190 are assigned slots in this area for data in accordance with their requests and with the priorities given by the cable modem termination system 42 to these requests. Optionally, the cable modem transmit opportunity region 176 may be considered as having two sub-regions. In a sub-region 178, slots

are specified for individual subscribers on the basis of requests of a high priority. Slots are specified in an area 180 for individual subscribers on the basis of requests of a low priority.

The frame 118 may optionally also include a maintenance region 182. This corresponds to the maintenance region 116 in FIG. 4. As previously described, the region 182 provides for a time coordination in the clock signals of the cable modem termination system 42 and the cable modems 190. The frame 118 additionally may optionally include a region 184 in the contention data region 168 where a collision has occurred. Valid data is provided in an area 186 in the frame where no collision occurred. A blank or empty area 188 may exist at the end of the contention data region 186 where further data could be inserted, subject to potential collisions. It will be appreciated that the different regions in the frame 118, and the sequence of these different regions, are illustrative only and that different regions and different sequences of regions may alternatively be provided.

The signals of the frames 118 from different cable modems 190a, 190b, 190c, 190d, etc. (FIG. 10) are introduced in upstream data processing through a common line 191 (FIGs. 9 and 10) to a TDMA demultiplexer 192 (FIG. 9) in the cable modem termination system 42. After demultiplexing, data in from the cable modems 190a, 190b, 190c, 190d, etc. pass from the demultiplexer 192 to a data interface 194. The signals at the data interface 194 are processed in an Ethernet system (not shown) or the like. The operation of the MAP generator 198 is controlled by data requests from the individual cable modems 190a, 190b, 190c, 190d, etc. and by collision information which is indicative of the cable modems 190a, 190b, 190c, 190d, etc. attempts to insert data in the contention data region 168. Thus, for example, a large number of collision may indicate a need for a larger contention request region 172 in the next MAP. Attempts to insert data in the contention data region 168 may, optionally, be utilized by the MAP generator 198 to increase the priority of any cable modem unsuccessfully attempting to transmit such data. The MAPs generated by the MAP generator 198 pass through the multiplexer 196 and are broadcast by the cable modem termination system 42 to the cable modems 190a, 190b, 190c, 190d.

A sample MAP generated by the MAP generator 198 is generally indicated at 202 in FIG. 9. The MAP 202 includes a region 204 where the requests of the cable modems 190 for Information Elements (IE) within which to transmit data are indicated. As previously indicated, an Information Element (IE) may be considered to be the same as a region. The MAP 202 also includes a region 206 where the cable modem termination system 42 has granted the requests of the subscribers for Information Elements to transmit data. The MAP 202 additionally includes a contention data region 208 where the cable modem termination system 42 has given the cable modems 190 the opportunity to transmit data in available spaces or slots without specifying the open spaces or slots where such transmission is to take place. An acknowledgment region 210 is also included in the MAP 202. In this region, the cable modem termination system 42 acknowledges to the cable modem 190 that it has received data from the subscribers in the available slots in the contention data region 208. As discussed above, the cable modem termination system 42 has to provide such acknowledgment because the cable modems 190 will

not otherwise know that the cable modem termination system 42 has received the data from the cable modems 190 in the contention data region 208.

Referring now to FIGs. 11-18, different aspects of an improved system in which the cable modems 190 and the cable modem termination system 42 cooperate to fragment packets of the data transmitted from the cable modems 190 to the cable modem termination system 42 are shown. FIG. 11 specifically shows a complete one of the extended packets 118. The extended packet 118 is indicated in a block form at 118a to show schematically the length of the extended packet. Details of the extended packet are indicated at 118b in FIG. 11. As shown, the extended packet 118b includes a header portion 500. The header portion 500 may be further defined by fields constituting a frame control (FC) 502, a fragmentation MAC Header (PARM) 504 and a total length (LEN) 506 of the extended packet. The functions of the fields 502, 504 and 506 and the specific implementation of these fields in binary coding are shown in FIG. 15.

The extended packet 118b includes an extended length field or segment (EHDR) 508 which indicates the length of the data in the extended data packet and which provides for the performance of a number of additional functions shown in FIG. 16. For example, the field 508 may include flags to indicate the first and last fragments in the packet 118b when the packet is fragmented.

The extended packet 118b may also include a MAC Header Check Sequence (HCS) 510 which consists of 2 bytes and which insures the integrity of the sequence in the header in a known manner. The header check sequence 510 is followed by data 512 (the complete payload) in the extended packet 118b. The data 512 is shown in cross-hatched lines in FIG. 10. A cyclic redundancy check (CRC) 514 follows the payload 512. A cyclic redundancy check such as 514 is known in the prior art to provide an additional check for insuring that the information in the packet 118b is complete.

FIG. 12 is a schematic diagram of a concatenation of a number of complete extended packets (such as that of FIG. 11) provided by one of the cable modems 190. The concatenation is indicated by a concatenation header 520 which is followed by the information for the first of the extended packets in the concatenation. This information includes a header (MAC HDR1) 522 for the first one of the concatenated packets, a payload (PDU) 524 for the first one of the concatenated packets and a cyclic redundancy check 526 for the first one of the concatenated packets. Similar information is provided for the successive ones of the extended packets in the concatenation. The last one (the nth) of the extended packets in the concatenation is indicated by a MAC header (MAC HDR_n) 530, a payload (PDU_n) 532 and a cycle redundancy check (CRC_n) 534. The payload 524 and 532 are indicated in cross-hatched lines.

FIG. 13 is a schematic diagram of a plurality of data packet fragments transmitted from the cable modem 190 to the cable modem termination system 42, wherein the data packet fragments form, in composite, a complete data packet. FIG. 13 schematically shows different fragmentary portions, generally indicated at 540a, 540b and 540c, of a complete packet such as the complete packet 118b in FIG. 11. Each of the fragments 540a, 540b and 540c includes a fragmentation header 542, a fragmentation header check sequence 544, a fragmentation payload

546 and a fragmentation check redundancy cycle 548. Thus, the fragmentation payloads 540a, 540b and 540c form, in composite, the complete payload for the packet 118.

Each of the fragmentation headers 542 includes a frame control (FC) 541, a segment (EHDR LEN) 543 indicating the length of the fragmentation header 542, a length segment (LEN) 545 indicating the length of the fragmentation header 542 and an extended header (EHDR) 547 containing additional information about the fragment.

FIG. 14 shows the fragmentation portion 540a in additional detail. As shown in FIG. 14, the fragmentation portion 540a includes the frame control (1 byte) 541, a MAC_PARM (1 byte) 543, the indication (LEN) (2 bytes) 545, the extended header (EHDR) 542, the header check sequence (HCS) 544, the payload fragment 546 and the fragment cyclic redundancy check (FCRC) 548. The MAC_PARM 543 indicates the length of the EHDR 542.

The frame control 541 is shown in FIG. 14 as including an FC type 566. The FC type 566 indicates a media access controller (MAC) specific header. The FC PARM 568 provides a fragmentation MAC header. The EHDR-ON 570 indicates that a fragmentation EHDR follows. The MAC PARM 543 indicates the length of the fragmentation EDHR. LEN indicates the total length of the fragment including the payload, EHDR and FCRC.

The EHDR portion 556 may be considered as including an extended header_type (EH_Type) segment 572 which indicates the type of data in the fragmentation portion 540a. For example, the type of information in the fragmentation portion 540a may constitute unencrypted fragmentation data or encrypted fragmentation data. Another segment in the EHDR portion is indicated at 574 and is designated as EH_LEN. It indicates the length of the EHDR. An additional segment 576 is designated as EH Value. It provides different types of information. For example, it includes a binary bit (or flag) which is set to a binary 1 to indicate a first fragment for the payload in the extended packet 118a and another bit (or flag) which is set to a binary 1 to indicate the last fragment for the payload in the extended packet. These bits are provided with a binary 0 for intermediate data fragments between the first data fragment and the last data fragment in the extended packet 118a. These flags for the fragments shown in FIG. 13 would be F=1, L=0 for 540a, F=0, L=0 for 540b, and F=0, L=1 for 540c. The segment 576 also includes a sequence number which is incremented for each fragment of a packet. This sequence number can be set to zero for the first fragment within a packet or continue counting from the last fragment of the last packet transmitted for this modem. This sequence number is used by the cable modem termination system to detect lost fragments during packet reassembly.

FIGs. 15 and 16 provide a table indicating, in a first column, the different types of fields shown in FIG. 14. FIGs. 15 and 16 also include a second column designated as Usage. This column indicates the different sub-fields (if any) shown in FIGs. 11-14 for the different fields specified in the first column of FIGs. 15 and 16 and specifies the operations in such sub-fields. The number of bits in the sub-fields is indicated in a third column in FIGs. 15 and 16. The number of bytes is specified for each of the fields specified in the first column of FIG. 11 and is shown in a fourth column in FIG. 16.

FIGs. 17 and 18 define a flowchart, generally indicated at 600, in block form and show how the cable modem 190 and the cable modem termination system 42 cooperate in the

fragmentation of the payload 118b for packets transmitted by the cable modem 190 to the cable modem termination system 42. The operation of the blocks in the flowchart 600 is initiated at a start block 602. As indicated at block 604 in FIG. 17, the cable modem 190 then awaits a packet from an external source. For example, the external source may be a personal computer (PC) 48 (FIG. 3) at the home 14 of a subscriber. As shown in block 606, the cable modem 190 then submits to the cable modem termination system 42 a bandwidth request for enough time slots to transmit the packet. Upon receipt of the request, the cable modem termination system sends a grant or partial grant to the cable modem in the MAP.

The cable modem 190 then checks as at block 610 to determine if the cable modem termination system 42 has granted the request, or any portion the request, from the cable modem 190. In block 610, SID is an abbreviation of Service Identification. If the answer is Yes (see line 611 in FIGs. 17 and 18), the cable modem 190 then determines if the cable modem termination system 42 has granted the full request from the cable modem 190 for the bandwidth. This corresponds to the transmission of the complete data packet from the cable modem 190 to the cable modem termination system 42. This is indicated at block 612 in FIG. 18.

If the answer is Yes, as indicated at block 614 in FIG. 18, the cable modem 190 determines if there is another packet in a queue which is provided to store other packets awaiting transmission to the cable modem termination system 42 from the cable modem 190. This determination is made at block 616 in FIG. 17. If there are no other packets queued, as indicated on a line 617 in FIGs. 17 and 18, the cable modem 190 sends the packet without a piggyback request to the cable modem termination system 42 (see block 618 in FIG. 17) and awaits the arrival of the next packet from the external source as indicated at 604. If there are additional packets queued as indicated by a line 619 in FIGs. 17 and 18, the cable modem 190 sends to the cable modem termination system 42 the packet received from the external source and piggybacks on this transmitted packet a request for the next packet in the queue. This is indicated at 620 in FIG. 17. The cable modem then returns to processing MAPs at 608 looking for additional grants. The cable modem termination system 42 then processes the next request from the cable modem.

The cable modem termination system 42 may not grant the full request for bandwidth from the cable modem 190 in the first MAP 111. The cable modem termination system 42 then provides this partial grant to the cable modem 190. If the CMTS operates in multiple grant mode, it will place a grant pending or another grant in the MAP in addition to the partial grant it sends to the cable modem. The cable modem processes the MAPs as shown in 608 and sees the grant in 611. The grant is smaller than the request as on 622 so the cable modem calculates the amount of the packet that will fit in the grant as on 624. With a multiple grant mode CMTS, the cable modem will see the partial grant with an additional grant or grant pending in subsequent MAPs as in 610 and 611. The cable modem then sends the fragment, without any piggyback request as in 628 and 630 to the cable modem termination system 42.

The cable modem return to processing map information elements in 608 until it gets to the next grant. The cable modem then repeats the process of checking to see if the grant is large enough as in 612.

If the next grant is not large enough, the cable modem repeats the process of fragmenting the remaining packet data and, as in 626, checking to see if it needs to send a piggyback request based on additional grants or grant pendings in the MAP.

If the grant is large enough to transmit the rest of the packet as on 614, the cable modem checks to see if there is another packet enqueued for this same SID. If so, the cable modem sends the remaining portion of the packet with the fragmentation header containing a piggyback request for the amount of time slots needed to transmit the next packet in the queue as on line 620. The cable modem then returns to processing the MAP information elements. IF there is not another packet enqueued for this SID, then the cable modem sends the remaining portion of the packet with fragmentation header containing no piggyback request as shown in 618. The cable modem then returns to 604 to await the arrival of another packet for transmission.

When the cable modem termination system 42 partially grants the request from the cable modem 190 in the first MAP 11 and fails to provide an additional grant or grant pending to the cable modem 190 in the first MAP, the cable modem will not detect additional grants or grant pendings as on 632. The cable modem 190 then sends to the cable modem termination system 42 a fragment of the data packet and a piggyback request for the remainder as in 634. When the cable modem has transmitted the fragment with the piggybacked request as shown on line 638, the cable modem returns to processing MAP information elements as in 608 while waiting for additional grants. When the cable modem termination system receives the fragment with the piggybacked request, the cable modem termination system must decide whether to grant the new request or send a partial grant based on the new request. This decision is based on the scheduling algorithms implemented on the cable modem termination system.

Any time during the request/grant process, the cable modem termination system could fail to receive a request or the cable modem could fail to receive a grant for a variety of reasons. As a fail safe mechanism, the cable modem termination system places an acknowledgment time, or ACK time, in the MAPs it transmits. This ACK time reflects the time of the last request it has processed for the current MAP. The cable modem uses this ACK time to determine if its request has been lost. The ACK timer is said to have "expired" when the cable modem is waiting for a grant and receives a MAP with an ACK time later in time than when the cable modem transmitted its request. As the cable modem is looking for grants at 610, if the ACK time has not expired as on 644, the cable modem returns to processing the MAPs as in 608. If the ACK timer does expire as on 646, the cable modem checks to see how many times it has retried sending the request in 648. If the number of retries is above some threshold, the retries have been exhausted as on 654 and the cable modem tosses any untransmitted portion of the packet at 656 and awaits the arrival of the next packet. If the ACK timer has expired and the number of retries have not been exhausted as in 650, the cable modem uses a contention request region to transmit another request for the amount of time slots necessary to transmit the untransmitted portion of the packet as in 652. The cable modem then returns to processing the MAPS.

Reference is made to FIGS. 20 and 21 for a description of another embodiment of the invention. In this embodiment, there are wireless transmission links between homes 14 and HFC network 42. Each of homes 14 is equipped with radio frequency modem (RFM) 2000. A base

station 2002 is in wireless RF contact with RFM's 2000. The wireless architecture is similar to a cellular phone system. Code division multiple access (CDMA) transmission could be used between RFM's 2000 and base station 2002. Base station 2002 is connected by a fiber 2004 to a CMTS hub 2006. Hub 2006 is part of HFC network 42. Otherwise the components in FIGS. X and Y are the same, and bear the same reference numerals, as those described in connection with FIGS. 2 and 3. As illustrated in FIG. 21, CMTS hub 2006 can be integrated in the same cable system that also services CM's connected by fiber to hub 22. Thus, upstream and/or downstream channels can be installed in a home without physically laying cable all the way to the home. If desired, the downstream channel could be fiber because of the large bandwidth requirement, and the upstream channel could be wireless because there is a smaller bandwidth requirement.

The described functions of cable modems 46 could be carried out on a single integrated circuit chip as illustrated in FIG. 22. In this chip the output of an RF transmitter 3000 feeds the upstream channels of HFC network 42. The downstream channels of HFC network 42 feed the input of an RF receiver 3002. A time division multiple access (TDMA) controller 3004 is connected to the input of transmitter 3000. The output of receiver 3002 is connected to TDMA controller 3004. An ethernet 3006 serves as an interface between TDMA controller 3004 and a PC or other binary signal processing device. TDMA controller 3004 could be an application specific circuit or a microprocessor programmed to perform the described CMTS functions, including fragmentation. It is understood that the exemplary data packet fragmentation described herein and shown in the drawings represents only presently desired embodiments of the invention. Indeed, various modifications and additions may be made to such embodiments without departing from the spirit and scope of the invention. For example, requests to transmit data from cable modems need not be received by the cable modem termination system and the MAP need not be generated by the cable modem termination system, but rather requests may be received by an autonomous device, which operates independently of the cable modem termination system, and the MAPs may be generated by this or another autonomous device. Thus, these and other modifications and additions may be obvious to those skilled in the art and may be implemented to adapt the present invention for use in a variety of different applications.

Network Data Transmission Synchronization System and Method

The detailed description set forth below in connection with the appended drawings is intended as a description of the presently preferred embodiment of the invention and is not intended to represent the only form in which the present invention may be constructed or utilized. The detailed description sets forth the construction and functions of the invention, as well as the sequence of steps for operating the invention in connection with the illustrated embodiment. It is to be understood, however, that the same or equivalent functions may be accomplished by different embodiments (in either hardware or software) that are also intended to be encompassed within the spirit and scope of the invention.

The network data transmission synchronization system and method of the present invention are illustrated in FIGS. 1-8, which depict a presently preferred embodiment thereof.

Referring now to FIG. 1, the present invention includes a headend or cable modem termination system (CMTS) 10 which communicates with a plurality of cable modems (CMs) 12. Although only one cable modem 12 is shown in FIG. 1 for clarity, the cable modem termination system 10 actually communicates bidirectionally with a plurality of such cable modems 12. Such communication as discussed herein may actually occur between the cable modem system and the plurality of cable modems by communicating simultaneously with the cable modems on a plurality of separate frequency channels.

This invention primarily addresses communication of a plurality of different cable modems on a single frequency channel in a serial or time division multiplexing fashion, wherein the plurality of cable modems communicate with the cable modem termination system sequentially. However, it will be appreciated that while this plurality of cable modems is communicating on one channel with the cable modem termination system (using time division multiple access or TDMA), many other cable modems may be simultaneously communicating with the same cable modem termination system on a plurality of different channels (using frequency division multiplexing/time division multiple access or FDM/TDMA)

In a typical cable modem system, a single cable modem termination system 10 will typically communicate with between 250 and 500 cable modems. Thus, the cable modem system of the present invention includes a plurality of cable modems, each of which is substantially identical to the cable modem 12 of FIG. 1. Thus, although the following description generally discusses the operation of a single cable modem termination system and a single cable modem, those skilled in the art will appreciate that a plurality of cable modem termination systems and cable modems may similarly be utilized.

The cable modem 10 communicates with each of the cable modems 12 via a cable plant 14, which typically includes a hybrid fiber coaxial (HFC) network in which optical fiber facilitates communication from the cable modem termination system 10 to a plurality of hubs, each of which distribute signals from the optical fiber to a plurality of coaxial cables. Each hub may be located at a distance of up to approximately 100 miles from either the cable modem termination system 10 or from the next hub along the optical fiber.

Optionally, a plurality of cable modem termination systems may be synchronized with respect to one another so as to facilitate communication between any desired cable modem termination system and any desired cable modem(s).

According to one aspect of the present invention, the cable modem termination system 10 includes a crystal oscillator timing reference 16 which provides an output to a linear counting sequence generator 18. It is this timing reference 16 to which each of the cable modems 12 must be synchronized. The linear counting sequence generator 18 is incremented by the output of the crystal oscillator timing reference 16 and maintains a count representative of the number of cycles provided by the crystal oscillator timing reference 16 since the linear counting sequence generator 18 was last reset. According to the present invention, the linear counting sequence generator 18 includes a free-running counter having a sufficient count capacity to count for several minutes before resetting.

A timebase message generator 20 receives the count of the linear counting sequence generator 18 to provide an absolute time reference 21 which is inserted into the downstream information flow 22 provided by downstream data queue 24, as discussed in detail below. The timebase message generator 20 prefers a module function, i.e., a saw tooth pattern as a function of time) and the counter clock is generated by the oscillator with very tight accuracy.

Timing offset generator 26 receives a ranging signal message 27 from each individual cable modem 12 with which the cable modem termination system is in communication. The slot timing offset generator 26 provides a slot timing offset 28 which is representative of a slot timing offset between the cable modem termination system 10 and the cable modem 12 and inserts the slot timing offset 28 into the downstream information flow 22. The slot timing offset 28 is calculated by determining the position of the slot timing offset from the expected time 27 within a dedicated timing slot of the upstream communications, as discussed in detail below. The timing effort generator 26 encodes the timing offset (ranging error) detected by the upstream receiver into a slot timing offset message.

Slot timing offset messages are sent only after the frequency of the local reference clock has been acquired by the cable modem.

Downstream modulator 30 primarily modulates the downstream information flow 22. Absolute time references 21 are inserted at quasi-periodic intervals as determined by a timestamp send counter (FIG. 3, item 31). A slot timing offset message 28 is inserted after measuring the slot timing error upon the arrival of a ranging signal message 27.

The time line 32 of the cable modem termination system 10 shows that the slot timing offset 28 is the difference between the expected receive time and the actual receive time of the slot timing offset message 27.

According to one embodiment of the present invention, each cable modem 12 includes a downstream receiver 34 for facilitating demodulation of the data and timestamp message, and timing recovery of downstream communications from the cable modem termination system 10. The output of the downstream receiver 34 is provided to timebase message detector 36 and slot timing offset detector 38. The downstream information (any data communication, such as a file transfer or MPEG video signal) received by the downstream receiver 34 is also available for further processing, as desired.

The timebase message detector 36 detects the timebase message generated by timebase message generator 20 of the cable modem termination system 10. Similarly, the slot timing offset detector 38 detects the slot timing offset 28 generated by the slot timing offset generator 26 of the cable modem termination system 10. The timebase message detector 36 provides an absolute time reference 40 which is representative of the frequency of the crystal oscillator timing reference 16 of the cable modem termination system 10. The absolute time reference 40 is provided to a digital tracking loop 42 which provides a substantially stable clock output for the cable modem 12 which corresponds closely in frequency to the frequency of the crystal oscillator timing reference 16 of the cable modem termination system 10. Thus, the digital tracking loop 42 uses the absolute time reference 40, which is representative of the frequency of the crystal oscillator timing reference 16, to form an oscillator drive signal which drives a numerically

controlled oscillator 44 in a manner which closely matches the frequency of the crystal oscillator timing reference 16 of the cable modem termination system 10, as discussed in detail below.

A difference between the absolute time reference 40 and the output of a local time reference 46, which is derived from the numerically controlled oscillator 44, is formed by differencing circuit 48. This difference defines a frequency error value which represents the difference between the clock of the cable modem 12 (which is provided by local time reference 46) and the clock of the cable modem termination system 10 (which is provided by crystal oscillator timing reference 16).

This frequency error value is filtered by loop averaging filter 50 which prevents undesirable deviations in the frequency error value from affecting the numerically controlled oscillator 44 in a manner which would decrease the stability thereof or cause the numerically controlled oscillator 44 to operate at other than the desired frequency. The loop filter 50 is configured so as to facilitate the rapid acquisition of the frequency error value, despite the frequency error value being large, and then to reject comparatively large frequency error values as the digital tracking loop 42 converges, i.e., as the output of the local timing reference 46 becomes nearly equal to the absolute time reference 40, thereby causing the frequency error value to approach zero.

According to one embodiment of the present invention, an initial slot timing offset 52 is added by summer 54 to the output of the local time reference 46 to provide a partially slot timing offset corrected output 56. The partially slot timing offset corrected output 56 of summer 54 is then added to slot timing offset 58 provided by slot timing offset detector 38 to provide slot timing offset and frequency corrected time reference 60. The timing offset correction block is a simple adder which adds two message values. Such simplified operation is facilitated only when the resolution of the timing offset message is equal to or finer than that of the timestamp message.

The initial slot timing offset 52 is merely an approximation of the expected slot timing offset likely to occur due to the propagation and processing delays, whose approximate values have been predetermined. After frequency conversion using the phase locked loop and timebase message error, the slot timing offset 58 provides a final correction which is calculated by the cable modem termination system 10 in response to the cable modem termination system 10 receiving communications from the cable modem 12 which are not properly centered within their desired timing slots, as discussed in detail below.

Scaler 62 scales the frequency corrected time reference 60 so as to drive upstream transmitter 69 at the desired slot timing.

Time reference 64 is compared to the designated transmit time 66 which was allocated via downstream communication from the cable modem termination system 10 to the cable modem 12. When the time reference 64 is equal 67 to the designated transmit time, then an initiate burst command 68 is issued and the upstream data queue 70 is modulated to form upstream transmission 72.

The timing offset (error) message is generated by the cable modem termination system. The timing offset (error) is simply the difference between the expected time and the actual arrival time of the ranging message at the cable modem termination system (or Headend) burst receiver.

Referring now to FIG. 2, the cable modem termination system 10 and the cable modem 12 are described in further detail. The multiplexer 29 of the cable modem termination system 10 combines downstream information flow 22 with slot timing offset 28 from slot timing offset generator 26 and with absolute time reference 21 from timebase message generator 20 to provide downstream communications to the downstream transmitter, which includes downstream modulator 30 (FIG. 1).

The slot timing offset generator 26 receives a slot timing offset information 28 from the upstream receiver 25. The value of the slot timing offset defines the need, if any, to perform a slot timing offset correction at the cable modem.

The headend tick clock 15 includes the crystal reference 16 of FIG. 1 and provides a clock signal to linear count sequence generator 18. Slot/frame time generator 19 uses a clock signal provided by count sequence generator 18 to provide both an upstream message clock 21 and a receive now signal 23. The minislot clock 21 is the clock by which the message slots are synchronized to effect time division multiple access (TDMA) communications from each cable modem 12 to the cable modem termination system 10. A Transmit now signal is generated at the beginning of each minislot of a transmission at the cable modem. A Receive now signal is similarly generated at the beginning of a received packet at the cable modem termination system.

A minislot is a basic medium access control (MAC) timing unit which is utilized for allocation and granting of time division multiple access (TDMA) slots. Each minislot may, for example, be derived from the medium access control clock, such that the minislot begins and ends upon a rising edge of the medium access control clock. Generally, a plurality of symbols define a minislot and a plurality of minislots define a time division multiple access slot.

The cable modem 12 receives downstream data from the downstream channel 14B. A timebase message detector 36 detects the presence of a timebase message 21 in the downstream data.

Slot timing offset correction 47 is applied to upstream communications 14A prior to transmission thereof from the subscriber cable modem 12. The slot timing offset correction is merely the difference between the actual slot timing offset and the desired slot timing offset. Thus, the slot timing offset correction is generated merely by subtracting the actual slot timing offset from the desired offset. Slot/frame timing generator 49 transmits the upstream data queue 70 (FIG. 1) at the designated transmit time 66 (FIG. 1).

Summer 48 subtracts from the timebase message 21 of the local time reference 46 and provides an output to a loop filter 50 which drives numerically controlled oscillator 44, as discussed in detail below.

Upstream transmitter 11 facilitates the transmission of upstream communications 14A from the subscriber cable modem 12A and upstream receiver 13A facilitates the reception of the upstream communications 14A by the cable modem termination system 10.

Downstream transmitter 17 facilitates the transmission of downstream communications 14 from the cable modem termination system 16 to the cable modem 12 where downstream receiver 15 facilitates reception thereof.

Referring now to FIG. 3, the cable modem termination system 10 is shown in further detail.

As discussed above, the crystal oscillator timing reference 16 provides an output to linear counting sequence generator 18 which increments to provide a count representative of the frequency of the crystal oscillator timing reference 16. The counter 18 also provides a substantially jitterless headend reference which provides a clock signal for downstream data transmissions from the cable modem termination system 10. The jitterless headend reference is synchronized to the downstream symbol rate via synchronizer 37 which includes counters 90, 91, 92, inverter 93 and AND gate 94 which cooperate according to well-known principles to provide a timestamp latch enable to AND gate 39 to enable latch 41.

The linear counting sequence generator 18 provides its count to latch 41. Latch 41 provides the count from the linear counting sequence generator 18 to multiplexer 45 when an enable is provided to latch 41. The enable is provided to latch 41 when the synchronizer 37 provides a high output and the downstream processor 47 provides a low output to AND gate 39. The count from the linear counting sequence generator 18 is combined with a timebase message header 43 by multiplexer 45 and the combined count and timebase message header is provided to the downstream processor 47. The downstream processor 47 provides a control signal 49 to the multiplexer 45 to cause the multiplexer 45 to provide the count from the linear counting sequence generator 18 and the timebase message header 43 to the downstream processor 47 only when the downstream processor 47 is ready to insert the count and the timebase message header 43 into a downstream data communication.

Binary up counter 31 functions as a timestamp send timer so as to cause the count or absolute time reference 21 (FIG. 1) from the linear counting sequence generator 18 to be inserted into a downstream communication in a generally periodic fashion. The binary up counter 31 receives a count from the linear counting sequence generator 18. When the count of the binary up counter 31 equals a value stored in the threshold register 33, equality comparitor 35 provides a request timestamp send to the downstream processor 47. It is important to note that the timestamp includes the absolute time reference 21 (FIG. 1).

However, the downstream processor 47 does not immediately insert every combined count and timebase message header from multiplexer 45 into a downstream communication when the request timestamp send 59 is provided by the equality comparitor 35 to the downstream processor 47. Rather, the downstream processor 47 waits until any downstream message presently being transmitted is finished so as to prevent undesirable fragmentation thereof.

The downstream processor 47 provides downstream data, including downstream communications from the downstream data queue 49, a count from the linear counting sequence generator 18, and a timebase message header 43 from multiplexer 45 to the downstream modulator 51, which modulates the data, count, and timebase message header to form a downstream data communication 53 which includes a plurality of individual messages 55. Some

of these individual messages 55 includes communicated data such as file transfers and MPEG video and some of these messages 55 include timestamps and/or slot timing offsets to facilitate synchronization of a selected cable modem 12 with the cable modem termination system 10.

In this manner, a count which is representative of the frequency of the crystal oscillator timing reference 16 is transmitted from the cable modem termination system 10 to each cable modem 12.

A clock divider 19 selects a net from a vector of the output of the linear counting sequence generator 18 and provides a frequency reduced slow tick clock output signal.

Referring now to FIG. 4, an exemplary timing recovery circuit of a cable modem is shown in further detail. Downstream demodulator 95, which forms a portion of downstream receiver 15 of FIG. 2, provides clock and data signals which are derived from downstream communications 14B (FIG. 2). The data signals include downstream bytes which in turn include the count or timestamp 97 and timebase message header 81 transmitted by the cable modem termination system 10. Slot timing offset messages are included in the downstream flow of downstream data.

Timestamp detector 80 detects the presence of a timestamp header 81 among the downstream bytes and provides a timestamp arrived signal 82 which functions as a downstream byte clock sync. The timestamp arrived signal 82 is provided to synchronizer 83 which includes register 101, register 102, AND gate 103, inverter 104 and latch 105. Synchronizer 103 synchronizes the timestamp arrived signal 82 to the clock of the cable modem 12, to provide a data path enable tick clock sync 107 for enabling the digital tracking loop 42.

When the digital tracking loop 42 is enabled by the data path enable tick clock sync 107 output from the synchronizer 83 in response to detecting a timestamp header by timestamp detector 80, then the timestamp, which is a count provided by the linear counting sequence generator 18 of FIG. 3, is provided to the digital tracking loop 42 and the digital tracking loop 42 is enabled so as to process the timestamp.

A differencing circuit or saturating frequency detector 109 compares the timestamp to a count provided to the saturating frequency detector 109 by timebase counter 111 which is representative of the frequency of numerically controlled oscillator 44. The saturating frequency detector 109 provides a difference signal or frequency error value 112 which is proportional to the difference between the frequency of the numerically controlled oscillator 44 of the cable modem and the crystal oscillator reference 16 of the cable modem termination system.

If the difference between the value of the timestamp and the count of timebase counter 111 is too large, indicating that the timestamp may be providing an erroneous value, then the saturating frequency detector 109 saturates and does not provide an output representative of the difference between the value of the timestamp and the count of timebase counter 111. In this manner, erroneous timestamps are not accepted by the digital tracking loop 42.

Pass 113 loop enable allows the difference provided by the saturating frequency detector 109 to be provided to latch 115 when a global enable is provided thereto. The global enable is provided to zero or pass 113 when functioning of the digital tracking loop 42 is desired.

Latch 115 provides the frequency error value 112 to a loop filter which includes multipliers 117 and 119, scalers 121 and 123, summers 124, 125 and latch 127.

The multipliers 117 and 119 include shift registers which effect multiplication by shifting a desired number of bits in either direction. Scalers 121 and 123 operate in a similar manner.

The loop filter functions according to well-known principles to filter out undesirable frequency error values, such that they do not adversely affect the stability or operation of numerically controlled oscillator 44. Thus, the loop filter tends to smooth out undesirable deviations in the frequency error value signal, so as to provide a more stable drive signal for the numerically controlled oscillator 44.

According to one embodiment of the present invention, the multipliers 117 and 119 can be loaded with different coefficients such that the bandwidth of the loop filter may be changed from a larger bandwidth during initial acquisition to a smaller bandwidth during operation. The larger bandwidth used initially facilitates fast acquisition by allowing frequency error values having larger deviations to be accepted. As the digital tracking loop 42 converges, the frequency error value tends to become smaller. At this time, frequency error values having larger deviations would tend to decrease stability of the digital tracking loop 42 and are thus undesirable. Therefore, different coefficients, which decrease the bandwidth of the loop filter, are utilized so as to maintain stability of the digital tracking loop 42.

A table showing an example of coarse and fine coefficients K0 and K1 which are suitable for various different update rates and bandwidths are shown in FIG. 5.

The output of the loop filter is provided to latch 131. The output of latch 131 is added to a nominal frequency by summer 133 so as to define a drive signal for numerically controlled oscillator 44.

Those skilled in the art will appreciate that the addition of a frequency offset, if properly programmed to a normal frequency, will decrease the loop's acquisition time. This is due to the fact that the final value of the accumulator 127 will be closer to its initial value.

The nominal frequency is generally selected such that it is close in value to the desired output of the numerically controlled oscillator 44. Thus, when the numerically controlled oscillator 44 is operating at the desired frequency, the filtered frequency error value provided by latch 131 is nominally zero.

Referring now to FIG. 6, the software level of control occurs within a local processor and affects the digital tracking loop 42 via register writes to the loop filters linear and integrator coefficients. The loop filter's linear coefficient is that coefficient placed in multiplier 117 and the loop filter's integrator coefficient is that coefficient placed in multiplier 119. Loading different sets of coefficients into loop filter changes the loop filter's bandwidth, as discussed above.

Thus, coarse coefficients give the digital tracking loop 42 a relatively large bandwidth, which enables quick acquisition of frequency error values, while narrower loop bandwidths reject frequency error values representative of noisier variations in the error metric, thereby smoothing the digital tracking filter's 42 response. It is important to note that smooth response of the digital

tracking loop 42 is important in achieving low jitter between the cable modem 12 and the cable modem termination system 10.

According to the present invention before enabling the hardware acquisition control, the first stage of software acquisition control includes estimation 300 of the timestamp interarrival time, which is particularly estimated by averaging the timestamp interarrival time over a plurality, e.g., 5 to 50 arrivals. This estimation is important because the coarse and fine coefficients are obtained from the table shown in FIG. 5, where they are dependent upon the update rate, i.e., timestamp interarrival time.

After interarrival time is estimated 300, then the software controller enters an initialization state 301 wherein a trial counter (which counts the number of acquisition attempts thus far) is reset, the tracking loop 42 is disabled and the latch 127 of the loop integrator is reset.

Next, the trial counter is incremented and checked 303 to see if the number of acquisition attempts is less then a predetermined threshold. If the threshold is exceeded, then the controller goes back and performs interarrival estimation again. Otherwise, coarse coefficients are loaded 305 into the multipliers 117 and 119 of the digital tracking loop 42 and the loop is enabled. The software controller then waits 307 for the same number of timestamps to arrive as will the hardware controller, after which the sync bit that comes from the hardware controller is checked 309 to determine whether or not coarse lock has been achieved.

If sync is active (is equal to 1, then fine loop coefficients are loaded 310 and a programmable amount of time is allowed to lapse 311 before a sync bit is checked once again. The track error threshold is used to determine whether or not the tracking loop 42 is receiving timestamps which are suitable for updating the frequency of the numerically controlled oscillator 44. Failure 315 of coarse lock to be achieved causes the trial count to increment and further attempts to reacquire force lock can be made. Failure 315 of fine lock causes the acquisition process to be restarted and also resets the trial counter. It is assumed that if fine lock has been achieved, then the interarrival estimation should be accurate.

Referring now to FIG. 7, a more detailed-level control flow is shown to achieve frequency lock (or sync = 1). After starting 200, the cable modem 12 first waits 201 for the loop or data path enable 107 (FIG. 4) before becoming active. After the first timebase message 202 arrives, then the first timebase message 202 is loaded 203 into the timebase counter 111 (FIG. 4) of the digital tracking loop 42. This allows the digital tracking loop 42 to be initiated with a value which produces a zero frequency error value, so as to facilitate faster acquisition and prevent undesirable swings in the output of the numerically controlled oscillator 44. Thus, when the data path enable 107 is detected by the digital tracking loop 42, then the next arriving timestamp is loaded into the timebase counter of the cable modem 12 and the digital tracking loop 42 then waits 204 for the next timebase message to arrive.

Loading 203 of the initial timebase message into the timebase counter 111 enhances acquisition time because it forces the counter 111 of the cable modem 12 to have a value close to that of the linear counting sequence generator 18 of the cable modem termination system 10. When the next timebase message arrives 204, the number of messages that have arrived thus far

are compared 205 to a programmable threshold. If the number of messages (acquisition count) is less than the programmable threshold (acquisition threshold), then the acquisition count is incremented 206. If the number of messages received so far (acquisition count) is greater than the programmable threshold (acquisition threshold), then the current timebase error is checked 207 against an error threshold to determine whether or not sync can be declared (sync=1). If the timebase error is below the threshold, then hardware lock has been achieved and sync becomes active. The cable modem 12 then waits for the next timebase message to arrive. If the new timebase error exceeds the error threshold, then the cable modem 12 returns to the initial or start state 200, resets the acquisition count and the loop integrator value, i.e., the value stored in latch 127, and the acquisition process begins again.

Referring now to FIG. 8, a slot timing offset between the clock of the cable modem 12 and the clock of the cable modem termination system 10 must be determined so as to assure that messages transmitted by the cable modem 12 are transmitted during time slots allocated by the cable modem system 10. As those skilled in the art will appreciate, propagation delays 400 and processing delays 402 combine to cause the cable modem 12 to actually transmit at a later point in time than when it is requested to do so by the cable modem termination system 10. Thus, a slot timing offset must be provided to each cable modem 10, to assure that it transmits at the correct time.

This slot timing offset is determined by the cable modem termination system 12 by having the cable modem termination system 12 monitor a dedicated slot with enough guard time (ranging slot) in upstream communications so as to determine the slot timing error between the expected time and the actually arrived (or detected) time. Thus, the cable modem termination system 10 may use this error to cause the cable modem 12 to transmit at an earlier point in time so as to compensate for propagation and processing delays. This slot timing offset correction is roughly equal to 2Tpg plus Tprocess.

Generally, communications will be initialized utilizing a comparatively large guard time. After acquisition, when slot timing accuracy has been enhanced, then the guard time may be reduced substantially, so as to provide a corresponding increase in channel utilization efficiency.

It is understood that the exemplary network data transmission synchronization system and method described herein and shown in the drawings represents only a presently preferred embodiment of the invention. Indeed, various modifications and additions may be made to such embodiment without departing from the spirit and scope of the invention.

It will be appreciated that acquisition control, particularly as discussed and illustrated with respect to FIGs. 6 and 7, may be performed either by software, hardware, or any desired combination thereof.

Thus, these and other modifications and additions may be obvious to those skilled in the art and may be implemented to adapt the present invention for use in a variety of different applications.

Burst Receiver for Cable Modem System

The detailed description set forth below in connection with the appended drawings is intended as a description of an exemplary embodiment of the invention and is not intended to represent the only form in which the present invention may be constructed or utilized. The detailed description sets forth the construction and functions of the invention, as well as the sequence of steps for operating the invention in connection with the illustrated embodiment. It is to be understood, however, that the same or equivalent functions may be accomplished by different embodiments (in either hardware or software) that are also intended to be encompassed within the spirit and scope of the invention.

The present invention is discussed in relation to FIGs. 1-24 below, wherein FIG. 1 provides a general overview of the present invention, FIGs. 2-11 provide a description of synchronization (which is helpful for an appreciation of rapid acquisition, and FIGs. 12-24 provide a description of rapid acquisition.

Referring now to FIG. 1, an enhanced data packet acquisition burst receiver 500 includes an analog front-end such as an analog-to-digital converter 502 which receives analog data packets from an upstream channel and which converts the analog data packets into digital data packets, a fractional symbol timing loop 504 which determines a fractional symbol timing correction and applies the fractional symbol timing correction to the data packets, a carrier phase correction loop 506 which determines a carrier phase correction and applies the carrier phase correction to the data packets, a phase derotator 508 which corrects phase errors in the symbols of the data packets, and a conventional coherent amplitude estimator 510 which provides an amplitude correction by a conventional estimation process and applies the amplitude correction to the data packets via multiplier 512 prior to the data packets being provided to slicer 514. This process is described in detail below.

Referring now to FIG. 2, a hybrid fiber coaxial (HFC) network 1010 facilitates the transmission of data between a headend 1012, which includes at least one cable modem termination system, and a plurality of homes 1014, each of which contains a cable modem. Such hybrid fiber coaxial networks are commonly utilized by cable providers to provide Internet access, cable television, pay-per-view and the like to subscribers.

Approximately 500 homes 1014 are in electrical communication with each node 1016, 1034 of the hybrid fiber coaxial network 1010, typically via coaxial cable 1029, 1030, 1031. Amplifiers 1015 facilitate the electrical connection of the more distant homes 1014 to the nodes 1016, 1034 by boosting the electrical signals so as to desirably enhance the signal-to-noise ratio of such communications and by then transmitting the electrical signals over coaxial conductors 1030, 1031. Coaxial conductors 1029 electrically interconnect the homes 1014 with the coaxial conductors 1030, 1031, which extend between amplifiers 1015 and nodes 1016, 1034.

Each node 1016, 1034 is electrically connected to a hub 1022, 1024, typically via an optical fiber 1028, 1032. The hubs 1022, 1024 are in communication with the headend 1012, via optical fiber 1020, 1026. Each hub is typically capable of facilitating communication with approximately 20,000 homes 1014.

The optical fiber 1020, 1026 extending intermediate the headend 1012 and each hub 1022, 1024 defines a fiber ring which is typically capable of facilitating communication between approximately 100,000 homes 1014 and the headend 1012.

The headend 1012 may include video servers, satellite receivers, video modulators, telephone switches and/or Internet routers 1018, as well as the cable modem termination system. The headend 1012 communicates via transmission line 1013, which may be a T1 or T2 line, with the Internet, other headends and/or any other desired device(s) or network.

Referring now to FIG. 3, a simplified block diagram shows the interconnection of the headend 1012 and an exemplary home 1014, wherein a cable modem 1046 communicates with a cable modem termination system, embodied as a line card 1042, via hybrid fiber coaxial network 1010.

More particularly, a personal computer 1048, disposed within the home 1014, is connected via cable 1011 to the cable modem 1046 which communicates via coaxial cable 1017 with the hybrid fiber coaxial network 1044, which in turn communicates via optical fiber 1020 with the line card or cable modem termination system (CMTS) 1042 of the headend 1012. Internet router 1040 facilitates communication between the headend 1012 and the Internet or any other desired device or network.

Referring now to FIG. 4, the present invention includes a cable modem termination system 10 (defined by line card 42 of FIG. 3) which communicates with a plurality of cable modem's timing circuits 12. The timestamp generation at the CMTS and the upstream timing recovery logic at the CM, and the flow of timestamp message are shown in this figure. Although only one cable modem 12 is shown in FIG. 4 for clarity, the cable modem termination system 10 actually communicates bidirectionally with a plurality of such cable modems 12. Such communication as discussed herein may actually occur between the cable modem system and the plurality of cable modems by communicating simultaneously with the cable modems on a plurality of separate frequency channels.

This invention primarily addresses communication of a plurality of different cable modems on a single frequency channel in a serial or time division multiplexing fashion, wherein the plurality of cable modems communicate with the cable modem termination system sequentially. However, it will be appreciated that while this plurality of cable modems is communicating on one channel with the cable modem termination system (using time division multiple access or TDMA), many other cable modems may be simultaneously communicating with the same cable modem termination system on a plurality of different channels (using frequency division multiplexing/time division multiple access or FDM/TDMA)

In a typical cable modem system, a single cable modem termination system or line card 1042 (FIG. 3) will typically communicate with between 250 and 500 cable modems 1046. Thus, the cable modem system of the present invention includes a plurality of cable modems 1046. Although the following description generally discusses the operation of a single cable modem termination system 1042 and a single cable modem 1046, those skilled in the art will appreciate that a plurality of cable modem termination systems 1042 and cable modems 1046 may similarly be utilized.

The cable modem termination system 10 communicates with each of the cable modems 12 via a cable plant 14, which typically includes a hybrid fiber coaxial (HFC) network in which optical fiber facilitates communication from the cable modem termination system 10 to a plurality of hubs, each of which distribute signals from the optical fiber to a plurality of coaxial cables. Each hub may be located at a distance of up to approximately 100 miles from either the cable modem termination system 10 or from the next hub along the optical fiber.

Optionally, a plurality of cable modem termination systems may be synchronized with respect to one another so as to facilitate communication between any desired cable modem termination system and any desired cable modem(s).

According to one aspect of the present invention, the cable modem termination system 10 includes a crystal oscillator timing reference 16 which provides an output to a linear counting sequence generator 18. It is this timing reference 16 to which each of the cable modems 12 must be synchronized. The linear counting sequence generator 18 is incremented by the output of the crystal oscillator timing reference 16 and maintains a count representative of the number of cycles provided by the crystal oscillator timing reference 16 since the linear counting sequence generator 18 was last reset. According to the present invention, the linear counting sequence generator 18 includes a free-running counter having a sufficient count capacity to count for several minutes before resetting.

A timebase message (timebase message and timestamp message are used interchangeably herein) generator 20 receives the count of the linear counting sequence generator 18 to provide an absolute time reference 21 which is inserted into the downstream information flow 22 provided by downstream data queue 24, as discussed in detail below. The timebase message generator 20 performs a module function, i.e., a sawtooth pattern as a function of time) and the counter clock is generated by the oscillator with very tight accuracy.

Slot timing offset generator 26 receives a timing offset message 27 from each individual cable modem 12 with which the cable modem termination system is in communication. The slot timing offset generator 26 provides a slot timing offset 28 which is representative of a slot timing offset between the cable modem termination system 10 and the cable modem 12 and inserts the slot timing offset 28 into the downstream information flow 22. The slot timing offset 28 is calculated by determining the position of the slot timing offset from the expected time 27 within a dedicated timing slot of the upstream communications, as discussed in detail below. The timing offset generator 26 encodes the timing offset (ranging error) detected by the upstream receiver into a message form.

Slot timing offset messages are sent only after the frequency of the local reference clock has been acquired by the cable modem.

Downstream modulator 30 primarily modulates the downstream information flow 22. Absolute time references 21 are inserted at quasi-periodic intervals as determined by a timestamp send counter (FIG. 3, item 31). A slot timing offset 28 is inserted shortly after the arrival of a slot timing offset message 27.

The time line 32 of the cable modem termination system 10 shows that the slot timing offset 28 is the difference between the expected receive time and the actual receive time of the slot timing offset message 27.

According to one embodiment of the present invention, each cable modem 12 includes a downstream receiver 34 for facilitating demodulation of the data and timestamp message, and timing recovery of downstream communications from the cable modem termination system 10. The output of the downstream receiver 34 is provided to timebase message detector 36 and slot timing offset detector 38. The downstream information (any data communication, such as a file transfer or MPEG video signal) received by the downstream receiver 34 is also available for further processing, as desired.

The timebase message detector 36 detects the timebase message generated by timebase message generator 20 of the cable modem termination system 10. Similarly, the slot timing offset detector 38 detects the slot timing offset 28 generated by the slot timing offset generator 26 of the cable modem termination system 10. The timebase message detector 36 provides an absolute time reference 40 which is representative of the frequency of the crystal oscillator timing reference 16 of the cable modem termination system 10. The absolute time reference 40 is provided to a digital tracking loop 42 which provides a substantially stable clock output for the cable modem 12 which corresponds closely in frequency to the frequency of the crystal oscillator timing reference 16 of the cable modem termination system 10. Thus, the digital tracking loop 42 uses the absolute time reference 40, which is representative of the frequency of the crystal oscillator timing reference 16, to form an oscillator drive signal which drives a numerically controlled oscillator 44 in a manner which closely matches the frequency of the crystal oscillator timing reference 16 of the cable modem termination system 10, as discussed in detail below.

A difference between the absolute time reference 40 and the output of a local time reference 46, which is derived from the numerically controlled oscillator 44, is formed by differencing circuit 48. This difference defines a frequency error value which represents the difference between the clock of the cable modem 12 (which is provided by local time reference 46) and the clock of the cable modem termination system 10 (which is provided by crystal oscillator timing reference 16).

This frequency error value is filtered by loop averaging filter 50 which prevents undesirable deviations in the frequency error value from affecting the numerically controlled oscillator 44 in a manner which would decrease the stability thereof or cause the numerically controlled oscillator 44 to operate at other than the desired frequency. The loop filter 50 is configured so as to facilitate the rapid acquisition of the frequency error value, despite the frequency error value being large, and then to reject comparatively large frequency error values as the digital tracking loop 42 converges, i.e., as the output of the local timing reference 46 becomes nearly equal to the absolute time reference 40, thereby causing the frequency error value to approach zero.

According to one embodiment of the present invention, an initial slot timing offset 52 is added by summer 54 to the output of the local time reference 46 to provide a partially slot timing offset corrected output 56. The partially slot timing offset corrected output 56 of summer 54 is

then added to slot timing offset 58 provided by slot timing offset detector 38 to provide slot timing offset and frequency corrected time reference 60. The timing offset correction is a simple addition which adds two message values. Such simplified operation is facilitated only when the resolution of the timing offset message is equal to or finer than that of the timestamp message.

The initial slot timing offset 52 is merely an approximation of the expected slot timing offset likely to occur due to the propagation and processing delays, whose approximate values have been predetermined. After frequency conversion using the phase locked loop and timebase message error, the slot timing offset 58 provides a final correction which is calculated by the cable modem termination system 10 in response to the cable modem termination system 10 receiving communications from the cable modem 12 which are not properly centered within their desired timing slots, as discussed in detail below.

Scaler 62 scales the frequency corrected time reference 60 so as to drive upstream transmitter 69 at the desired slot timing.

Time reference 64 is compared to the designated transmit time 66 which was allocated via downstream communication from the cable modem termination system 10 to the cable modem 12. When the time reference 64 is equal 67 to the designated transmit time, then an initiate burst command 68 is issued and the upstream data queue 70 is modulated to form upstream transmission 72.

The timing offset (error) message is generated by the cable modem termination system. The timing offset (error) is simply the difference between the expected time and the actual arrival time of the message during the ranging slot at the cable modem termination system receiver.

Referring now to FIG. 5, the cable modem termination system 10 and the cable modem 12 are described in further detail. The multiplexer 29 of the cable modem termination system 10 combines downstream information flow 22 with slot timing offset 28 from slot timing offset generator 26 and with absolute time reference 21 from timebase message generator 20 to provide downstream communications to the downstream transmitter, which includes downstream modulator 30 (FIG. 4).

The slot timing offset generator 26 receives a slot timing offset signal 28 from the upstream receiver 25. The location of the slot timing offset signal within a timing slot of an upstream communication defines the need, if any, to perform a slot timing offset correction. Generally, a slot timing offset value will be transmitted, even if the actual slot timing offset is 0. When the slot timing offset message is desirably located within the timing offset slot, and does not extend into guard bands which are located at either end of the timing offset slot, then no slot timing offset correction is necessary.

However, when the slot timing offset message extends into one of the guard bands of the timing offset slot of the upstream communication, then a slot timing offset 28 is generated by the slot timing offset generator 26, which is transmitted downstream to the cable modem 12 where the slot timing offset 28 effects a desired correction to the time at which upstream communications occur, so as to cause the slot timing offset message and other transmitted data to be positioned properly within their upstream data slots.

The headend tick clock 15 includes the crystal reference 16 of FIG. 4 and provides a clock signal to linear counting sequence generator 18. Slot/frame time generator 19 uses a clock signal provided by count sequence generator 18 to provide both an minislot clock 21 and a receive now signal 23. The upstream message clock 21 is the clock by which the message slots are synchronized to effect time division multiple access (TDMA) communications from each cable modem 12 to the cable modem termination system 10. A Transmit_now signal is generated at the beginning of each minislot of a transmission. A Receive_now signal is similarly generated at the beginning of a received packet.

A minislot is a basic medium access control (MAC) timing unit which is utilized for allocation and granting of time division multiple access (TDMA) slots. Each minislot may, for example, be derived from the medium access control clock, such that the minislot begins and ends upon a rising edge of the medium access control clock. Generally, a plurality of symbols define a minislot and a plurality of minislots define a time division multiple access slot.

The cable modem 12 receives downstream data from the downstream channel 14B. A timebase message detector 36 detects the presence of a timebase message 21 in the downstream data.

Slot timing offset correction 47 is applied to upstream communications 14A prior to transmission thereof from the subscriber cable modem 12. The slot timing offset correction is merely the difference between the actual slot timing offset and the desired slot timing offset. Thus, the slot timing offset correction is generated merely by subtracting the actual slot timing offset from the desired offset. Slot/frame timing generator 49 transmits the upstream data queue 70 (FIG. 4) at the designated transmit time 66 (FIG. 4).

Summer 48 subtracts from the timebase message 21 of the local time reference 46 and provides an output to a loop filter 50 which drives numerically controlled oscillator 44, as discussed in detail below.

Upstream transmitter 11 facilitates the transmission of upstream communications 14A from the subscriber cable modem 12A and upstream receiver 13A facilitates the reception of the upstream communications 14A by the cable modem termination system 10.

Downstream transmitter 17 facilitates the transmission of downstream communications 14 from the cable modem termination system 16 to the cable modem 12 where downstream receiver 15 facilitates reception thereof.

Referring now to FIG. 6, the cable modem termination system 10 is shown in further detail.

As discussed above, the crystal oscillator timing reference 16 provides an output to linear counting sequence generator 18 which increments to provide a count representative of the frequency of the crystal oscillator timing reference 16. The counter 18 also provides a substantially jitterless headend reference which provides a clock signal for downstream data transmissions from the cable modem termination system 10. The jitterless headend reference is synchronized to the downstream symbol rate via synchronizer 37 which includes counters 90, 91, 92, inverter 93 and AND gate 94 which cooperate according to well-known principles to provide a timestamp latch enable to AND gate 39 to enable latch 41.

The linear counting sequence generator 18 provides its count to latch 41. Latch 41 provides the count from the linear counting sequence generator 18 to multiplexer 45 when an enable is provided to latch 41. The enable is provided to latch 41 when the synchronizer 37 provides a high output and the downstream processor 47 provides a low output to AND gate 39. The count from the linear counting sequence generator 18 is combined with a timebase message header 43 by multiplexer 45 and the combined count and timebase message header is provided to the downstream processor 47. The downstream processor 47 provides a control signal 49 to the multiplexer 45 to cause the multiplexer 45 to provide the count from the linear counting sequence generator 18 and the timebase message header 43 to the downstream processor 47 only when the downstream processor 47 is ready to insert the count and the timebase message header 43 into a downstream data communication.

Binary up counter 31 functions as a timestamp send timer so as to cause the count or absolute time reference 21 (FIG. 4) from the linear counting sequence generator 18 to be inserted into a downstream communication in a generally periodic fashion. The binary up counter 31 receives a count from the linear counting sequence generator 18. When the count of the binary up counter 31 equals a value stored in the threshold register 33, equality comparitor 35 provides a request timestamp send to the downstream processor 47. It is important to note that the timestamp includes the absolute time reference 21 (FIG. 4).

However, the downstream processor 47 does not immediately insert every combined count and timebase message header from multiplexer 45 into a downstream communication when the request timestamp send 59 is provided by the equality comparitor 35 to the downstream processor 47. Rather, the downstream processor 47 waits until any downstream message presently being transmitted is finished so as to prevent undesirable fragmentation thereof.

The downstream processor 47 provides downstream data, including downstream communications from the downstream data queue 49, a count from the linear counting sequence generator 18, and a timebase message header 43 from multiplexer 45 to the downstream modulator 51, which modulates the data, count, and timebase message header to form a downstream data communication 53 which includes a plurality of individual messages 55. Some of these individual messages 55 includes communicated data such as file transfers and MPEG video and some of these messages 55 include timestamps and/or slot timing offsets to facilitate synchronization of a selected cable modem 12 with the cable modem termination system 10.

In this manner, a count which is representative of the frequency of the crystal oscillator timing reference 16 is transmitted from the cable modem termination system 10 to each cable modem 12.

A clock divider 19 selects a net from a vector of the of the output of the linear counting sequence generator 18 and provides a frequency reduced slow tick clock output signal.

Referring now to FIG. 7, an exemplary timing recovery circuit of a cable modem is shown in further detail. Downstream demodulator 95, which forms a portion of downstream receiver 15 of FIG. 5, provides clock and data signals which are derived from downstream communications 14B (FIG. 5). The data signals include downstream bytes which in turn include the count or timestamp 97 and timebase message header 81 transmitted by the cable modem

termination system 10. Slot timing offset messages are included in the downstream flow of downstream data.

Timestamp detector 80 detects the presence of a timestamp header 81 among the downstream bytes and provides a timestamp arrived signal 82 which functions as a downstream byte clock sync. The timestamp arrived signal 82 is provided to synchronizer 83 which includes register 101, register 102, AND gate 103, inverter 104 and latch 105. Synchronizer 103 synchronizes the timestamp arrived signal 82 to the clock of the cable modem 12, to provide a data path enable tick clock sync 107 for enabling the digital tracking loop 42.

When the digital tracking loop 42 is enabled by the data path enable tick clock sync 107 output from the synchronizer 83 in response to detecting a timestamp header by timestamp detector 80, then the timestamp, which is a count provided by the linear counting sequence generator 18 of FIG. 6, is provided to the digital tracking loop 42 and the digital tracking loop 42 is enabled so as to process the timestamp.

A differencing circuit or saturating frequency detector 109 compares the timestamp to a count provided to the saturating frequency detector 109 by timebase counter 111 which is representative of the frequency of numerically controlled oscillator 44. The saturating frequency detector 109 provides a difference signal or frequency error value 112 which is proportional to the difference between the frequency of the numerically controlled oscillator 44 of the cable modem and the crystal oscillator reference 16 of the cable modem termination system.

If the difference between the value of the timestamp and the count of timebase counter 111 is too large, indicating that the timestamp may be providing an erroneous value, then the saturating frequency detector 109 saturates and does not provide an output representative of the difference between the value of the timestamp and the count of timebase counter 111. In this manner, erroneous timestamps are not accepted by the digital tracking loop 42.

Pass 113 loop enable allows the difference provided by the saturating frequency detector 109 to be provided to latch 115 when a global enable is provided thereto. The global enable is provided to zero or pass 113 when functioning of the digital tracking loop 42 is desired.

Latch 115 provides the frequency error value 112 to a loop filter which includes multipliers 117 and 119, scalers 121 and 123, summers 124, 125 and latch 127.

The multipliers 117 and 119 include shift registers which effect multiplication by shifting a desired number of bits in either direction. Scalers 121 and 123 operate in a similar manner.

The loop filter functions according to well-known principles to filter out undesirable frequency error values, such that they do not adversely affect the stability or operation of numerically controlled oscillator 44. Thus, the loop filter tends to smooth out undesirable deviations in the frequency error value signal, so as to provide a more stable drive signal for the numerically controlled oscillator 44.

According to one embodiment of the present invention, the multipliers 117 and 119 can be loaded with different coefficients such that the bandwidth of the loop filter may be changed from a larger bandwidth during initial acquisition to a smaller bandwidth during operation. The larger bandwidth used initially facilitates fast acquisition by allowing frequency error values having larger deviations to be accepted. As the digital tracking loop 42 converges, the frequency

error value tends to become smaller. At this time, frequency error values having larger deviations would tend to decrease stability of the digital tracking loop 42 and are thus undesirable. Therefore, different coefficients, which decrease the bandwidth of the loop filter, are utilized so as to maintain stability of the digital tracking loop 42.

A table showing an example of coarse and fine coefficients K0 and K1 which are suitable for various different update rates and bandwidths are shown in FIG. 8.

The output of the loop filter is provided to latch 131. The output of latch 131 is added to a nominal frequency by summer 133 so as to define a drive signal for numerically controlled oscillator 44.

Those skilled in the art will appreciate that the addition of a frequency offset, if properly programmed to a normal frequency, will decrease the loop's acquisition time. This is due to the fact that the final value of the accumulator 127 will be closer to its initial value.

The nominal frequency is generally selected such that it is close in value to the desired output of the numerically controlled oscillator 44. Thus, when the numerically controlled oscillator 44 is operating at the desired frequency, the filtered frequency error value provided by latch 131 is nominally zero.

Referring now to FIG. 9, a flowchart showing the two levels of control, i.e., coarse lock and fine lock, of the digital tracking loop 42 (FIG. 7) is provided. As mentioned above, the coarse lock utilizes coefficients for the multipliers 117 and 119 which provide a large bandwidth of the loop filter which is suitable for the acquisition of the frequency error value so as to initiate tracking, while the fine coefficients provide enhanced stability of the numerically controlled oscillator 44, so as to prevent undesirable fluctuations in the output thereof. According to one exemplary embodiment of the present invention, a hardware control level, i.e., utilizing coarse coefficients for the multipliers 117 and 119, achieves a coarse frequency lock and then a software level changes the loop coefficients to achieve a final, low jitter frequency lock. At the hardware level, a state of frequency lock implies that the difference between arriving timebase message values and the clock, i.e., output of the numerically controlled oscillator 44, of the cable modem 12 is below a predetermined or programmable error threshold. Software lock implies that a final low jitter lock state has been achieved.

After starting 200, the cable modem 12 first waits 201 for the loop or data path enable 107 (FIG. 7) before becoming active. After the first timebase message 202 arrives, then the first timebase message 202 is loaded 203 into the timebase counter 111 (FIG. 7) of the digital tracking loop 42. This allows the digital tracking loop 42 to be initiated with a value which produces a zero frequency error value, so as to facilitate faster acquisition and prevent undesirable swings in the output of the numerically controlled oscillator 44. Thus, when the data path enable 107 is detected by the digital tracking loop 42, then the next arriving timestamp is loaded into the timebase counter of the cable modem 12 and the digital tracking loop 42 then waits 204 for the next timebase message to arrive.

Loading 203 of the initial timebase message into the timebase counter 111 enhances acquisition time because it forces the counter 111 of the cable modem 12 to have a value close to that of the linear counting sequence generator 18 of the cable modem termination system 10.

When the next timebase message arrives 204, the number of messages that have arrived thus far are compared 205 to a programmable threshold. If the number of messages (acquisition count) is less than the programmable threshold (acquisition threshold), then the acquisition count is incremented 206. If the number of messages received so far (acquisition count) is greater than the programmable threshold (acquisition threshold), then the current timebase error is checked 207 against an error threshold to determine whether or not sync can be declared (sync=1). If the timebase error is below the threshold, then hardware lock has been achieved and sync becomes active. The cable modem 12 then waits for the next timebase message to arrive. If the new timebase error exceeds the error threshold, then the cable modem 12 returns to the initial or start state 200, resets the acquisition count and the loop integrator value, i.e., the value stored in latch 127, and the acquisition process begins again.

Referring now to FIG. 10, the software level of control occurs within a local processor and affects the digital tracking loop 42 via register writes to the loop filters linear and integrator coefficients. The loop filter's linear coefficient is that coefficient placed in multiplier 117 and the loop filter's integrator coefficient is that coefficient placed in multiplier 119. Loading different sets of coefficients into loop filter changes the loop filter's bandwidth, as discussed above.

Thus, coarse coefficients give the digital tracking loop 42 a relatively large bandwidth, which enables quick acquisition of frequency error values, while narrower loop bandwidths reject frequency error values representative of noisier variations in the error metric, thereby smoothing the digital tracking filter's 42 response. It is important to note that smooth response of the digital tracking loop 42 is important in achieving low jitter between the cable modem 12 and the cable modem termination system 10.

According to the present invention, before enabling the hardware acquisition control, the first stage of software acquisition control includes estimation 300 of the timestamp interarrival time, which is particularly estimated by averaging the timestamp interarrival time over a plurality, e.g., 10 to 50 arrivals. This estimation is important because the coarse and fine coefficients are obtained from the table shown in FIG. 8, where they are dependent upon the update rate, i.e., timestamp interarrival time.

After interarrival time is estimated 300, then the software controller enters an initialization state 301 wherein a trial counter (which counts the number of acquisition attempts thus far) is reset, the tracking loop 42 is disabled and the latch 127 of the loop integrator is reset.

Next, the trial counter is incremented and checked 303 to see if the number of acquisition attempts is less then a predetermined threshold. If the threshold is exceeded, then the controller goes back and performs interarrival estimation again. Otherwise, coarse coefficients are loaded 305 into the multipliers 117 and 119 of the digital tracking loop 42 and the loop is enabled. The software controller then waits 307 for the same number of timestamps to arrive as will the hardware controller, after which the sync bit that comes from the hardware controller is checked 309 to determine whether or not coarse lock has been achieved.

If sync is active (is equal to 1, then fine loop coefficients are loaded 310 and a programmable amount of time is allowed to lapse 311 before a sync bit is checked once again.

The track error threshold is used to determine whether or not the tracking loop 42 is receiving timestamps which are suitable for updating the frequency of the numerically controlled oscillator 44. Failure 315 of coarse lock to be achieved causes the trial count to increment and further attempts to reacquire force lock can be made. Failure 315 of fine lock causes the acquisition process to be restarted and also resets the trial counter. It is assumed that if fine lock has been achieved, then the interarrival estimation should be accurate.

Referring now to FIG. 11, a slot timing offset between the clock of the cable modem 12 and the clock of the cable modem termination system 10 must be determined so as to assure that messages transmitted by the cable modem 12 are transmitted during time slots allocated by the cable modem system 10. As those skilled in the art will appreciate, propagation delays 400 and processing delays 402 combine to cause the cable modem 12 to actually transmit at a later point in time than when it is requested to do so by the cable modem termination system 10. Thus, a slot timing offset must be provided to each cable modem 10, to assure that it transmits at the correct time.

This slot timing offset is determined by the cable modem termination system 12 by having the cable modem termination system 12 monitor a dedicated slot timing offset slot in upstream communications so as to determine the position of a slot timing offset message therein. The position of the slot timing offset message within the dedicated slot timing offset slot in the upstream communication determines the slot timing offset between the clock of the cable modem termination system 10 and the clock of the cable modem 12. Thus, the cable modem termination system 10 may use this error to cause the cable modem 12 to transmit at an earlier point in time so as to compensate for propagation and processing delays. This slot timing offset correction is equal to 2Tpg plus Tprocess.

Initially, the slot timing offset slot includes a comparatively large time slot, i.e., having comparatively large guard times, so as to accommodate comparatively large slot timing offset error. In a normal data packet, the width of the timing offset slot may be reduced when slot timing offset errors become lower (thus requiring smaller guard bands), so as to facilitate more efficient upstream communications.

Generally, communications will be initialized utilizing a comparatively large guard time. After acquisition, when slot timing accuracy has been enhanced, then the guard time may be reduced substantially, so as to provide a corresponding increase in channel utilization efficiency.

According to a further aspect of the present invention, data packets are acquired rapidly, e.g., in an order of sixteen symbol or so, so as to facilitate enhanced efficiency of bandwidth usage. As those skilled in the art will appreciate, it is desirable to acquire data packets as fast as possible, so as to minimize the length of a header, preamble or other non-information bearing portion of the data packet which is used exclusively for such acquisition.

As used herein, acquisition is defined to include the modifications or adjustments made to a receiver so that the receiver can properly interpret the information content of data packets transmitted thereto. Any time spent acquiring a data packet detracts from the time available to transmit information within the data packet (because of the finite bandwidth of the channel), and is therefore considered undesirable.

According to the present invention, acquisition includes the performance of fine adjustments to the parameters which are defined or adjusted during the ranging processes. During the ranging processes, slot timing, carrier frequency, and gross amplitude (power) of the data packet are determined. During acquisition, these parameters are fine-tuned so as to accommodate fractional symbol timing, carrier phase correction and fine amplitude of the data packet.

Moreover, according to the present invention, a ranging process is used to control power, slot timing and carrier frequency in the upstream TDMA channel. Power must be controlled so as to provide normalized received power at the cable modem termination system, in order to mitigate inter-channel interference. The carrier frequency must be controlled so as to ensure proper channelization in the frequency domain. Slot timing must be controlled so as to mitigate the undesirable collision of data packets in the time domain and to account for differential propagation delays among different cable modems.

Fractional symbol timing is a precise modification to slot timing. In slot timing, the clocks of the cable modems are synchronized such that a data packet is transmitted within a slot defined by the cable modem termination system, so as to avoid collisions of data packets transmitted simultaneously by different cable modems. During acquisition, fractional symbol timing allows the receiver to sample symbols at the correct time. Thus, fractional symbol timing causes the receive symbols of the data packet to be aligned in time such that they are properly demodulated. As those skilled in the art will appreciate, it is important to detect the amplitude of QAM symbols at the correct time, so as to facilitate proper interpretation of the amplitude thereof.

Carrier phase correction is a fine tuning of carrier frequency correction, which is performed during the ranging process. Carrier phase correction is necessary in order for the phase derotator to properly compensate for phase errors in the received packet.

Fine amplitude correction is a more precise correction to gross amplitude correction, which is performed during a ranging process. Amplitude corrections must be applied to the incoming data packet, so as to assure that the amplitude is properly defined prior to amplitude detection by the slicer.

Thus, according to the present invention, acquiring a data packet in a cable modem termination system includes determining fractional symbol timing correction, determining carrier phase correction and determining fine amplitude correction. According to the present invention, fractional symbol timing correction is determined by a feedback loop process, carrier phase correction is determined by a loop process and fine amplitude correction is determined by an estimation process. Unlike conventional methodology where fractional symbol timing correction, carrier phase correction, and fine amplitude are all determined by an estimation or correlation technique, this architecture can take advantages of the following merits: a) the same feedback loops can be used both for acquisition and tracking of symbol timing and carrier phase, and b) the carrier phase acquisition and small frequency offset correction (important during the ranging process) can be performed by using the second-order loop architecture.

More particularly, the present invention includes determining fractional symbol timing correction via a fractional symbol timing phase locked loop which controls a phase of a signal representative of the data packet being acquired as the data packet is processed in a resampler which provides an input to a phase derotator and includes determining a carrier phase correction which is performed by a carrier phase correction phase locked loop which controls a phase of a signal representative of the data packet being acquired in the phase derotator. In this manner, the fractional symbol timing is controlled as the signal representative of the data packet being acquired is processed by the resampler and the carrier phase is controlled as the derotator performs phase correction.

The first resampler 1154 (shown in FIG. 22) provides a sample rate suitable for processing by a matched filter and/or the phase derotator. It allows the analog-to-digital converter sample rate and the symbol rate to be independent and also programmable by the resampling factor. Optionally, the matched filter processes the signal representative of the data packet being acquired before the resampler which provides a sample rate suitable for carrier phase recovery and a separate resampler 1146 (shown in FIG. 22) is used to perform fast clock phase recovery, as discussed in detail below.

The matched filter compensates for the effects produced by a shaping filter of the cable modem transmitter which provided the data packet being acquired, according to well-known principles.

Thus, according to one aspect of the present invention, the signal representative of the data packet being acquired is processed by a first resampler to provide a sample rate suitable for the matched filter. Then, a signal representative of the data packet being acquired is processed by the matched filter. Then, the signal representative of the data packet being acquired is processed by a second resampler to provide a sample rate suitable for the phase derotator which the phase of the signal representative of the data packet being acquired is processed by a phase derotator to effect correction of a phase of either the in-phase (I) or quadrature (Q) channel of a QAM signal while the phase of the signal representative of the data packet being acquired is controlled by a carrier phase correction phase locked loop. Then, the signal representative of the data packet being acquired is multiplied by an estimated amplitude correction factor to provide a signal suitable for processing by the slicer. Then, the signal representative of the data packet being acquired is processed by the slicer to effect demodulation of an amplitude component of the I or Q channel of the QAM signal.

Optionally, the input gain (or phase detector gain) of the fractional symbol timing phase locked loop and/or the carrier phase correction phase locked loop by sensing an amplitude input to a phase detector of the loop and modifying the amplitude of the input to the loop filter.

As those skilled in the art will appreciate, loop filters tend to be amplitude sensitive since the coefficients selected therefor may not be valid if the input to the phase detector has an amplitude which is substantially different from that for which the coefficients were selected. The use of coefficients which are not suitable for the input amplitude to the phase detector may therefore result in undesirably increased acquisition time of the signal being acquired.

According to the present invention, use of the fractional symbol timing feedback loop and the carrier phase loop with minimum loop delay, as well as the fine amplitude estimation process, facilitate the acquisition of a data packet having a preamble which is sixteen symbols or less in length.

According to the present invention, the preamble includes a binary pattern and a unique word (FIG. 17). Further, according to the present invention, both the binary pattern and the unique word are modulated using quadrature phase shift keying (QPSK). Thus, the entire preamble is modulated using QPSK.

The fractional symbol timing and the carrier phase are determined using the binary pattern of the preamble. The fine amplitude correction is determined using the unique word of the preamble.

According to one aspect of the present invention, as shown in FIG. 24, the fractional symbol timing acquisition is accelerated by utilizing two offset symbol sampling clocks and selecting that offset symbol sampling clock which provides samples having the highest absolute value at the beginning of each burst. As those skilled in the art will appreciate, when only a single symbol sampling clock is utilized, the phase of the symbol sampling clock may be such that samples of the alternating binary pattern are taken at times when the alternating binary pattern is near the transition point, i.e., has a value which is approximately zero, and the sample levels are therefore ambiguous or difficult to reliably determine.

Thus, when only one symbol sampling clock is utilized, the phase of that single symbol sampling clock must be varied until the alternating binary pattern is properly acquired. As those skilled in the art will appreciate, varying the phase of the single sampling clock until the alternating binary pattern is properly acquired (has sufficient amplitude) is undesirably time consuming and thus results in a greater acquisition time of the alternating binary pattern of the preamble.

The use of two offset symbol sampling clocks, particularly when the two offset symbol sampling clocks are offset approximately 180 degrees with respect to one another, inherently causes one of the two symbol sampling clocks to sample when the amplitude of the alternating binary pattern is sufficient to reliably determine the information content thereof. Thus, according to this aspect of the present invention, two offset symbol sampling clocks, each having a phase difference of approximately 180 degrees with respect to the other, are utilized and that clock which provides the best, e.g., highest amplitude (absolute value) is utilized in the sampling process for the alternating binary pattern of the preamble. The use of two offset symbol sampling clocks thus substantially shortens the acquisition time of the alternating binary pattern.

Referring now to FIG. 12, the cable modem termination system 42 (typically defined by the line card of FIG. 3) comprises a burst receiver 292 for receiving data packets in the upstream data flow, a continuous transmitter 290 for broadcasting to the cable modems 46 via the downstream data flow and a medium access control (MAC) 60 for providing an interface between the burst receiver 292, the continuous transmitter 290 and other headend communications devices such as video servers, satellite receivers, video modulators, telephone switches and Internet routers 1018 (FIG. 2).

Each cable modem 46 (FIG. 3) comprises a burst transmitter 294 for transmitting data to the cable modem termination system 42 via upstream data flow, a continuous receiver 296 for receiving transmissions from the cable modem termination system 42 via the downstream data flow and medium access control (MAC) 90 for providing an interface between the burst transmitter 294, the continuous receiver 296 and subscriber communications equipment such as a PC 48 (FIG. 3), a telephone, a television, etc.

The burst receiver 292, medium access control (MAC) 60 and continuous transmitter 290 of the cable modem termination system 42 and the burst transmitter 294, medium access control (MAC) 90 and continuous receiver 296 of each cable modem may each be defined by a single separate, integrated circuit chip.

Referring now to FIG. 13, the line card or cable modem termination system 42 of FIG. 3 is shown in further detail. The cable modem termination system 42 is configured to receive signals from and transmit signals to an optical fiber 79 of the hybrid fiber coax (HFC) network 1010 (FIG. 3) via optical-to-coax stage 49, which is typically disposed externally with respect to the line card or cable modem termination system 42. The optical-to-coax stage 49 provides an output to the 5-42 MHz RF input 56 via coaxial cable 54 and similarly receives a signal from the RF up converter 78 via coaxial cable 52.

The output of the RF input 56 is provided to splitter 57 of the cable modem termination system 42, which separates the 5-42 MHz RF input into N separate channels. Each of the N separate channels is provided to a separate QPSK/16-QAM burst receiver channel 58.

Each separate QPSK/16-QAM burst receiver channel 58 is in electrical communication with the headend MAC 60. The headend MAC 60 is in electrical communication with backplane interface 62 which provides an interface to ROM 70, RAM 68, CPU 66, and 100BASE-T Ethernet interface 64.

The headend MAC 60 provides clock and a data output to the downstream modulator 72 which provides an output to amplifier 76 through surface acoustic wave (SAW) filter 74. Amplifier 76 provides an output to 44 MHz IF output, which in turn provides an output to the RF upconverter 78.

Each burst receiver 58 is configured so as to be capable of receiving both QPSK (4-QAM) or 16-QAM signals. The QPSK signals provide 2 bits per symbol, wherein each bit has ± 1 amplitude levels. The 16-QAM signals provide 4 bits per symbol, each bit having a ± 1 or ± 3 amplitude level.

However, the description and illustration of a burst receiver configured to accommodate QPSK and 16-QAM inputs is by way of illustration only and not by way of limitation. Those skilled in the art will appreciate that other modulation techniques, such as 32-QAM, 64-QAM and 256-QAM may alternatively be utilized.

Referring now to FIG. 14, a contemporary, continuous transmission is shown wherein a series of contiguous payloads 1101, such as those defined by data packets, are concatenated to define a generally continuous data stream 1100. Because the data stream 1100 is generally continuous, e.g., does not contain periodic interruptions, acquisition only occurs infrequently, such as during startup or initialization.

The contemporary data stream 1100 as shown in FIG. 14 is suitable for point-to-point transmission, such as between a single transmitter and a single receiver.

Referring now to FIG. 15, data bursts 1105 define a discontinuous data stream 1103. The data bursts 1105 are typically defined by data packets and are separated by guard bands 1107. The area between guard bands 1107 where the data bursts 1105 are located is defined by a time division multiple access (TDMA) time slot which the cable modem termination system 42 is pre-assigned to cable modems 46 which have previously requested such time slots in order to facilitate upstream communications. The guard bands 1107 provide some tolerance between adjacent time slots, so as to mitigate the occurrence of undesirable data collisions between adjacent data packets.

It is possible, such as in light data traffic conditions, that one or more adjacent time slots might be empty, thereby further increasing the time between adjacent data bursts.

Because the data bursts 1105 are discontinuous, each data packet which defines a data burst 1105 must be reacquired by the burst receiver 58.

The discontinuous nature of such time division multiple access (TDMA) upstream communications is thus due to the fact that a plurality of different cable modems are competing for upstream channel bandwidth. Since the upstream channel is divided into a plurality of time slots, so as to accommodate the plurality of cable modems transmitting in the upstream channel, it is difficult, if not impossible, to define a single, continuous upstream data transmission.

Thus, the discontinuous nature of the upstream data communication necessitates the use of a burst receiver which is capable of re-acquiring each individual data packet.

Referring now to FIG. 16, the data packet which defines each data burst 1105 comprises a QPSK or QPSK-like preamble (i.e., a subset of 16-QAM constellations) 1109 and a 16-QAM payload 1110. The QPSK preamble 1109 is an order of sixteen symbols long. It is during this sixteen symbol QPSK preamble 1109 that acquisition by the burst receiver 58 takes place. It is during acquisition that fractional symbol timing correction, carrier phase correction and fine amplitude correction are determined, so as to facilitate proper and reliable demodulation of the 16-QAM payload 1110.

Referring now to FIG. 17, the QPSK preamble 1109 comprises a binary pattern 1111 (better shown in FIG. 24) and a unique word 1112. The binary pattern 1111 of the QPSK preamble 1109 is used in the recovery or acquisition of fractional symbol timing and carrier phase. The unique word is used in the recovery or acquisition of fine amplitude. The unique word also optionally provides an identification of the transmitting cable modem 46.

Fractional symbol timing correction and carrier phase correction are both determined by fast feedback loop processes. According to the present invention, fractional symbol timing correction is performed by a fractional symbol timing phase locked loop and carrier phase correction is performed by a carrier phase correction phase locked loop, both of which are discussed in detail below.

Referring now to FIG. 18, a contemporary phase locked loop 1120 comprises a phase detector 1122 to which a first signal is provided at input 1124. The signal provided to the first input 1124 is a signal having some degree of timing information. The timing of the signal

provided to input 1124 may not be stable and/or may not be comprised of well-defined, substantially noiseless pulses, such as those of an oscillator or a clock.

When it is desired to provide a comparatively stable, well-defined noiseless reference signal, such as that which may be used to facilitate sampling in an analog-to-digital converter, it is necessary to use the original signal to facilitate timing recovery.

The phase detector 1122 provides an output which is proportional to a difference in phase between the signal provided at input 1124 and a feedback signal provided at input 1125. Because the output of the phase detector 1122 typically comprises an undesirable high frequency component, loop filter 1127 is used to assure that only desirable low frequency components of the output of the phase detector 1122 are provided to voltage controlled oscillator 1129. The output of voltage controlled oscillator 1129 is provided as a reference signal or the second input 1125 to phase detector 1122. The output of voltage controlled oscillator 1129 also forms the desired comparatively stable, well-defined, substantially noise-free reference for use in such applications as clocking or sampling.

Referring now to FIG. 19, a simplified phase locked loop 1130a typically used in a digital receiver, which includes a matched filter 1131 in addition to the standard phase locked loop components of a loop filter 1132, a numerically controlled oscillator 1133 and phase detector 1134, is shown. The phase locked loop shown in FIG. 19 is a somewhat simplified version of the fractional symbol timing correction phase locked loop of FIG. 21, which likewise includes a matched filter.

It is important to understand that the matched filter 1131 of the simplified phase locked loop 1130 inherently represents an undesirable time delay, and thus, undesirably increases acquisition time of the phase locked loop 1130.

Referring now to FIG. 20, according to one aspect of the present invention (shown in detail in FIG. 22), the matched filter 1131 is moved outside of the phase locked loop 1130b so as to remove the undesirable time delay from the loop and thereby improve the acquisition time thereof. The phase locked loop shown in FIG. 20 is a somewhat simplified version of the fractional symbol timing correction phase locked loop of FIG. 22, wherein the matched filter has been moved outside of the phase locked loop.

Referring now to FIG. 21, according to one aspect of the present invention, a burst receiver circuit 1139a comprises a fractional symbol timing phase locked loop 1140a, a carrier phase correction phase locked loop 1141 and an amplitude estimator circuit 1142. As shown in FIG. 21, the matched filter 1145a of the fractional symbol timing phase locked loop 1140a is inside the phase locked loop defined by resampler 1146, phase detector 1147, loop filter 1148 and numerically controlled oscillator 1149. According to this aspect of the present invention, the matched filter 1145 introduces an undesirable time delay, thereby inhibiting fast acquisition of the fractional symbol timing.

The burst receiver 1139a shown in FIG. 21 includes an analog-to-digital converter 1150, a down converter which includes a direct digital frequency synthesizer 1151 and a mixer or multiplier 1152, and a low pass filter 1153 for removing unwanted high frequency components which result from the mixing process of the down converter.

The carrier phase correction phase locked loop 1141 includes the phase derotator 1160, phase detector 1161, loop filter 1162 and numerically controlled oscillator 1163, which operate as discussed above with respect to FIG. 18 so as to provide a phase reference signal to the phase derotator 1160 which corrects error in the carrier phase and small residual frequency error of the data packet which otherwise would tend to cause errors in the amplitude demodulation or slicing process.

Conventional coherent amplitude estimator circuit 1142 includes a conventional coherent amplitude estimator 1165 which operates according to well-known principles to provide an amplitude estimates or correction factor after fractional symbol timing and fine carrier frequency synchronization have been achieved.

The amplitude estimate or correction factor is applied to the data packet via multiplier 1166 before the data packet is input to equalizer 1170 which compensates for channel spectral deficiencies which would otherwise inhibit reliable amplitude demodulation by the slicer 1171.

Referring now to FIG. 22, burst receiver 1139b is identical to burst receiver 1139a with the exception that matched filter 1145b is outside of both phase locked loop 1140b, so as to avoid the undesirable inherent introduction of a delay in acquisition time caused by placing the matched filter 1145b within the timing recovery loop 1140a as shown in FIG. 21. Also, since the matched filter 1145b is placed ahead of resampler 1146 of the fractional symbol timing phase locked loop 1140b, a second resampler 1154 must be provided so as to provide the digitized data burst to the matched filter 1145b at a proper sample phase of the data.

Referring now to FIG. 23, phase detector gain boosting logic may optionally be provided so as to further enhance the speed at which acquisition occurs. As those skilled in the art will appreciate, the loop filter 1201 of a phase locked loop 1200 is sensitive to the amplitude of the signal provided thereto. That is, the coefficients selected for the loop filter 1201 must be appropriate for the amplitude of the signal provided to the loop filter 1201 in order to assure rapid acquisition of the signal input to the phase locked loop 1200.

In order to assure that the amplitude of the signal input to the loop filter 1201 is within a desired range, i.e., is appropriate for the coefficients selected for the low pass 1201, a sensor and amplitude control 1202 monitors the amplitude of the voltage input to phase detector 1203 and modifies, via mixer or multiplier 1204, the amplitude of the signal input to loop filter 1201 which provide an output to NCO 1205. Thus, when the amplitude of the signal input to the phase detector 1203 is too low, then the sensor and amplitude control 1202 increases the amplitude of the signal input to low pass 1201 such that the amplitude of the signal input to loop filter 1201 is within a desired range which is appropriate for the coefficients thereof. Similarly, when the sensor and amplitude control 1202 senses that the amplitude of the signal input to the phase detector 1203 is too high, then the sensor and amplitude control 1202 reduces the amplitude of the signal input to the low pass 1201, such that the amplitude of the signal input to the low pass 1201 is within the desired range for the coefficients of the loop filter 1201.

Referring now to FIG. 24, a timing recovery accelerator enhances the speed at which the binary preamble is acquired by assuring that the samples taken by the sampling circuit are taken at a time which assures reliable detection of the amplitude of the binary signal of the preamble.

According to contemporary practice, a single clock signal 1300 (waveform A) is used to clock the sample circuit (FIGs. 21 and 22) such that the sample circuit samples the binary preamble on the rising edge 1301 of the clock signal 1300, for example. However, in those instances when the rising edge 1301 occurs near the zero or transition point 1310 of the binary pattern 1111 preamble 1109, then the amplitude of the binary pattern 1111 may not provide high enough phase detector gain to facilitate reliable amplitude detection thereof to facilitate reliable amplitude detection thereof.

According to contemporary practice, when this occurs the clock for the sample circuit is shifted in phase until reliable detection of the amplitude of the binary preamble occurs. However, as those skilled in the art will appreciate, such shifting of the phase of the clock for the sample circuit is undesirably time consuming and thus, undesirably increases the acquisition time of the binary preamble.

The present invention uses two offset symbol sampling clocks 1302a and 1302b (waveform B). Both of the offset symbol sampling clocks 1302a and 1302b effect sampling by the sample circuit on the rising edges 1303a and 1303b, thereof respectively. The two offset symbol sampling clocks 1302a and 1302b are out-of-phase with one another, such as by 180 degrees. Therefore, at least one of the two offset symbol sampling clocks 1302a and 1302b must have a rising edge 1303a, 1303b which occurs when the amplitude of the binary preamble 1111 is near its maximum and can therefore be reliably detected.

According to the present invention, that offset symbol sampling clock which provides samples having the highest absolute value (to account for the negative voltage peaks) at the beginning of each burst (FIG. 24) is selected to provide a clock for the sample circuit. As those skilled in the art will appreciate, by utilizing two offset symbol sampling clocks and selecting that offset symbol sampling clock which provides the highest absolute value, the need to vary the phase of the symbol clock for the sampling circuit is eliminated and the speed at which acquisition is performed is substantially enhanced.

Thus, the present invention includes a receiver architecture having two resampler circuits. One is an open-loop resampler for the symbol clock frequency resampling and the other is a closed-loop resampler for symbol clock phase acquisition.

It is worthwhile to point out that two different power estimation processes may be performed by the burst receiver. The burst receiver may perform a narrow band power estimation and/or a wide band power estimation.

The narrow band power estimation relates to a particular symbol rate and is utilized to measure the narrow band channel noise power level, as a part of the channel estimate which is used to determine channel quality.

The wide band power estimate relates to the overall upstream band, typically from 5-42 MHz and may be used to determine the analog front-end gain setting. Generally, it is desired that

the analog front-end gain setting be configured to handle up to 50 dB of dynamic range at the upstream cable plant.

Referring now to FIG. 25, a wide gand RMS power estimator includes analog-to-digital converter 1350 which receives a wide band input. The analog-to-digital converter 1350 provides an output to absolute value block 1351 which takes the absolute value of the input thereto and provides an output to Leaky integrator 1352 which integrates the signal and provides an output to an able gate 1353.

The wide band RMS power estimator provides a coarse estimation which is used for initial variable gain amplifier setting.

A narrow band RMS power estimator is typically included after the Nyquist filters and provides an average power of the I and Q channels. According to an example embodiment, the narrow band RMS power estimator has a 2-byte output and a relatively large time constant, an order of tens of thousand symbols. Noise channel power estimation in an idle channel for spectrum management typically has a deviation of approximately 2 to 3 dB.

It is understood that the exemplary network data transmission synchronization system and method described herein and shown in the drawings represents only a presently preferred embodiment of the invention. Indeed, various modifications and additions may be made to such embodiment without departing from the spirit and scope of the invention. Thus, modifications and additions may be obvious to those skilled in the art and may be implemented to adapt the present invention for use in a variety of different applications.

Robust Techniques for Optimal Upstream Communication

The detailed description set forth below in connection with the appended drawings is intended as a description of an exemplary embodiment of the invention and is not intended to represent the only form in which the present invention may be constructed or utilized. The detailed description sets forth the construction and functions of the invention, as well as the sequence of steps for operating the invention in connection with the illustrated embodiment. It is to be understood, however, that the same or equivalent functions may be accomplished by different embodiments that are also intended to be encompassed within the spirit and scope of the invention.

The present invention specifically addresses and alleviates the above-mentioned deficiencies associated with the prior art. More particularly, the present invention provides a method for communicating information from a plurality of cable modems to a cable modem termination system which tends to optimize the data communication efficiency of the upstream channels.

According to one aspect, the present invention provides a technique in which a plurality of upstream channels are periodically monitored for at least one parameter which is indicative of channel quality. A first modulation method is used for each upstream channel for which the monitored parameter(s) indicate that channel quality is above a predetermined threshold value and a second modulation method is used for each upstream channel for which the monitored parameter(s) indicate that channel quality is below the predetermined threshold value. The first

modulation method utilizes a larger constellation size than the second modulation method, such that a higher data rate is achieved when the channel quality is good enough to support the higher data rate.

Further, the present invention provides in another aspect a method and apparatus for optimizing the efficiency of upstream data communications by dividing an upstream spectrum into a plurality of upstream channels, wherein each upstream channel has a bandwidth of less than or equal to approximately 0.5 MHz. The upstream channels are periodically monitored for at least one parameter which is indicative of the quality of each monitored upstream channel. Communications are moved from a used channel an unused channel when the monitored parameter(s) indicate that the quality of the used channel is below a predetermined threshold. In this manner, noisy channels tend to be avoided and communications occur on higher quality channels which are capable of supporting higher data rates.

The present invention in another aspect provides a method and apparatus for tending to optimize upstream communication efficiency wherein a communications channel having upper and lower frequency bounds is defined in an attempt to determine an optimal bandwidth of the channel given constraints imposed by the presence of adjacent channels, as well as constraints imposed by narrowband interference. Data rate is thus enhanced by varying the symbol rate of communications performed via the channel in a near-continuous manner, i.e., by varying the upper and/or lower frequency bounds, so as to enhance the bandwidth and thereby enhance the efficiency with which the available frequency spectrum is utilized.

Thus, according to the present invention, the data rate of the upstream channel tends to be optimized, so as to enhance the data communication efficiency of the upstream channel.

The present invention provides enhanced upstream data rates by utilizing a constellation which is efficient in view of transmission medium conditions, by providing fine frequency agility based upon channel quality monitoring so as to enhance the effectiveness with which the limited bandwidth of the upstream channel is utilized, and by providing nearly continuous symbol rate switching so as to facilitate the usage of an enhanced symbol rate which is compatible with line conditions.

The method and apparatus for communicating information from a plurality of cable modems to a cable modem termination system are illustrated in FIGs. 2 and 4-7, which depict certain exemplary embodiments thereof. FIGs. 1 and 3 depict prior art contemporary communications circuitry.

Referring now to FIG. 1, according to contemporary practice a cable modem termination system includes a plurality of demodulators 10A-10Z which receive modulated data which is input from a plurality of cable modems via a common transmission medium. The demodulators 10A-10Z provide a demodulated data output for the frequency division multiplexed (FDM) upstream channels via which data is transmitted from the plurality of cable modems to the cable modem termination system (CMTS). The cable modems communicate with the cable modem termination system via time division multiple access (TDMA), wherein a plurality of cable modems communicate with each demodulator 10A-10Z and wherein the cable modems

associated with each demodulator 10A-10Z are distinguished from those associated with a different demodulator via frequency division multiplexing (FDM).

Referring now to FIG. 2, according to the present invention monitoring circuit 12 of the cable modem system 36 monitors the ability of each FDM channel to reliably transmit data at a desired data rate. That is, a parameter which is indicative of channel quality is periodically monitored so as to determine the ability of the channel to facilitate upstream data communications. The channel monitoring function is, for example, incorporated into each individual burst receiver, of which there are typically eight per cable modem termination system. The averaging and statistic gathering function is may be common to all channels, and thus may reside separate from the individual burst receivers.

As used herein, channel quality is defined as the ability of a channel to transmit data reliably thereon, such that higher quality channels transmit data reliably at a higher data rate than lower quality channels.

When a quality of the channel, such as signal-to-noise (SNR) is determined to be above a predetermined threshold value, then a first modulation method is utilized for that upstream channel. When the quality of a channel is determined to be less than that of the predetermined threshold value, then a second modulation method is utilized. The first modulation method is capable of providing a higher data rate than the second modulation method. According to the illustrated embodiment of the present invention, first modulation method has a larger constellation size than the second modulation method. According to the exemplary embodiment of the present invention, the first modulation method encompasses 16-QAM and the second modulation method encompasses QPSK (4-QAM). Thus, according to the present invention, a constellation size is selected which is dependent upon transmission medium characteristics, such that the data rate of communications on each channel tends to be enhanced.

Alternatively, more than two different modulation methods may be utilized. Thus, a plurality of different modulation methods, wherein each individual modulation method is generally better suited for a different range of channel quality, may be utilized. In this manner, the efficiency of data communications is yet further enhanced.

The modulation method utilized for each upstream channel is communicated from the monitoring circuit 12 to each demodulator 14a-14z of the cable modem termination system and is also inserted into the downstream message flow such that the modulation method is communicated to each cable modem 30, thereby facilitating modulation by each cable modem with the desired modulation method.

Thus, each cable modem 30 includes a demodulator 32 for demodulating downstream data transmissions from the cable modem termination system 36 and also includes a modulator 34 for modulating upstream data transmissions. A central circuit 38 of the cable mode 30 controls the modulation method utilized by the modulator 34 and also controls the physical layer parameters such as forward error correcting gain and guard time.

According to one exemplary embodiment of the present invention, the step of periodically monitoring a plurality of channels contemplates periodically monitoring a signal-to-noise ratio for each of the monitored channels. The signal-to-noise ratios are monitored over a plurality of

separate communications bursts and an average of the signal-to-noise ratios is formed from the individual measurements. This average is compared to the predetermined threshold value so as to determine whether or not a change is to be made to the modulation method.

In an exemplary aspect of the invention, the predetermined signal-to-noise ratio threshold value is approximately 20 dB. Thus, if the signal-to-noise ratio is equal to or greater than 20 dB, then the first modulation method is utilized and when the signal-to-noise ratio is less than 20 dB, then the second modulation method is utilized.

In particular, the monitoring circuit 12 defines a portion of the cable modem termination system. Alternatively, the monitoring circuit 12 may be separate from the cable modem termination system, but might be located generally proximate thereto, such that an accurate assessment of each channel's ability to transmit data may be performed.

According to another exemplary embodiment of the present invention, the step of periodically monitoring a plurality of channels contemplates periodically monitoring channel noise power. Thus, channel noise power may be monitored and compared to a predetermined threshold value so as to determine which modulation method is to be utilized. Channel noise may be monitored in addition to signal-to-noise ratio (SNR) and/or any other desired parameter which is indicative of channel quality, such as channel statistics. Thus, any desired combination of parameters indicative of channel quality may be utilized according to the method of the present invention.

According to yet another exemplary embodiment of the present invention, the step of periodically monitoring a plurality of channels contemplates periodically monitoring channel statistics for each of the monitored upstream channels. Examples of the statistics which may be monitored for each upstream channel include the number of packets undetected, the number of packets with corrected errors, the number of packets with uncorrected errors, the number of forward error correction blocks with corrected errors, and the number of forward error correction blocks with uncorrected errors. Combinations of these criteria and/or other desired criteria may similarly be monitored. Thus, it will be appreciated that such channel statistics provide an indication of the quality of an upstream channel which may be utilized to determine which modulation method may be utilized to reliably and efficiently transmit data upon that channel.

Optionally, at least one physical layer parameter of a channel may be changed in response to a change in quality of the channel. For example, forward error correcting gain and/or the guard time associated with a channel may be changed in response to a change in the quality of the channel. This change in the physical layer parameter may be either in addition to or separate from any change in modulation methods.

Although periodic monitoring of one or more parameters indicative of channel quality is performed according to the exemplary embodiment of the present invention, those skilled in the art will appreciate that continuous monitoring at such parameters may alternatively be utilized, if desired.

Referring now to FIG. 3, a prior art method for receiving modulated data at a cable modem termination system from a transmission medium, such as a coaxial cable, and for

converting that received modulated data into digital data suitable for computer use includes demodulating the modulated data via an upstream burst receiver 11 and providing the demodulated data to medium access control (MAC) 13. Medium access control (MAC) 13 controls access of the cable modem termination system to the transmission medium and provides a digital data output representative of a message transmitted from a cable modem.

The upstream burst receiver is configured so as to be capable of demodulating both QPSK and 16-QAM modulation formats within a TDMA frame. According to contemporary methodology, the upstream burst receiver 11 is configured so as to demodulate modulated data from the transmission medium according to a single, predetermined modulation method. The predetermined modulation method must be selected such that it provides reliable data transmission for a wide range of transmission medium conditions. Of course, this necessitates that a modulation technique which provides reliable data transmission even under the worst expected transmission medium conditions must be utilized. As those skilled in the art will appreciate, such a modulation technique, QPSK for example, does not provide the enhanced data rates which may be possible when better medium conditions are present. That is, when only a single modulation method is utilized, then data rate must typically be sacrificed in order to provide the desired reliability.

Thus, in order to limit interruptions to upstream communications, cable modem systems typically utilize an upstream modulation method which is compatible with the lowest expected channel quality. However, as those skilled in the art will appreciate, such worst case modulation methods (QPSK, for example) are inherently inefficient at higher channel qualities. The modulation methods used for lower channel qualities provide reduced bit rates, while the modulation methodology suitable for higher channel qualities provide higher bit rates.

It is important to recognize that upstream data communications are characterized by a plurality of different time division multiplexed channels, wherein each individual channel originates from a different cable modem or a different group of cable modems. Because the transmission path between the cable modem termination system and each individual cable modem is not identical (even though a common coaxial cable may be utilized along some portion of the path), variations in channel quality occur. Thus, a wide variation in channel quality among channels, i.e., cable modems, is typical. These variations may occur because, for example, some of the cable modems and/or their links to the common coaxial cable are located proximate noise sources.

Referring now to FIG. 4, according to the present invention the cable modem termination system includes a spectrum management/allocation circuit 15 (as also shown in FIG. 2) which at least periodically monitors the plurality of upstream channels for at least one parameter which is indicative of channel quality. For example, spectrum management/allocation circuit 15 may receive signal-to-noise ratio or channel power values from the upstream burst receiver 11. Alternatively, the spectrum management/allocation circuit 15 receives packet/FEC status from a upstream MAC/PHY channel statistics circuit 12. The upstream MAC/PHY channel statistics circuit receives the output of the upstream burst receiver prior to the output of the upstream burst receiver being provided to the medium access control 13 and the upstream MAC/PHY channel

statistic circuit 12 calculates the packet/FEC statistics, which is then provided to spectrum management/allocation circuit 15.

Any desired combination of signal-to-noise ratio, channel power, packet statistics and/or forward error correction statistics may be utilized as the parameter which is indicative of channel quality.

Such monitoring of the signal-to-noise (SNR), channel power, and/or packet/FEC statistics facilitates the determination of which modulation method, e.g., QPSK or 16-QAM, is to be utilized as long as the quality of the channel is deemed to be sufficiently good to facilitate the use of such modulation methods. When the quality of the channel is insufficient to facilitate the use of the smallest constellation size, i.e., QPSK, then the spectral allocation of the channel is changed, as discussed in detail below.

Optional averaging circuit 17 averages a plurality of signal-to-noise (SNR) or channel power measurements to compensate for short term fluctuations therein.

When a change in modulation method is indicated, then the new modulation method is transmitted from a switch circuit 16 of the spectrum management/allocation circuit 15 to the upstream burst receiver 11 and is also transmitted to the affected cable modem via downstream message flow, as mentioned above.

When the quality of a channel is determined to be sufficiently poor (such that even QPSK will not provide reliable data transmission), then that channel may be moved to a different frequency allocation. When this occurs, the new upstream channel frequency is transmitted to the upstream burst receiver 11 and is also transmitted to the affected cable modem via downstream message flow.

A bandwidth selection circuit 19 of the spectrum management/allocation circuitry 15 thus facilitates the implementation of fine frequency agility and the switch 16. The bandwidth selection circuit 19 determines the bandwidth of each downstream channel and the switch 16 effects switching to the desired channel by the burst receiver 11. The upstream spectrum is divided into a plurality of upstream channels and wherein each channel is characterized as having a bandwidth which is less than or equal to 0.5 MHz.

According to the fine frequency agility aspect of the present invention, the spectrum management/allocation circuit 15 monitors the upstream channels for at least one parameter which is indicative of the quality of each monitored upstream channel and moves communications from a used channel to an unused channel when the monitored parameter indicates that the quality of the used channel is below a predetermined threshold value.

Thus, according to the present invention, 16-QAM is the baseline or default modulation method and QPSK is the fall-back modulation method, which is utilized only when channel quality is insufficient to support upstream data transmission utilizing 16-QAM. Channel reallocation is the fall-back method used when channel quality is insufficient for the use of QPSK.

The use of 16-QAM enhances channel band with efficiency by a factor of 2, typically from approximately 1.6 bits/Hz to approximately 3.2 bits/Hz, while providing approximately 25

percent excess bandwidth. For example, the use of 16-QAM provides up to 20.48 Mbps at 5.12 Mbaud.

However, it is important to appreciate that the detection of 16-QAM is much more difficult than the detection of QPSK, since the demodulation is amplitude sensitive, as well as phase sensitive when utilizing 16-QAM, whereas demodulation is only phase sensitive when utilizing QPSK.

It is expected that the above discussed combination of variable constellation size and fine frequency agility, i.e., dynamic channel allocation, will enhance channel bandwidth efficiency substantially.

It is important to understand that the upstream bandwidth in a hybrid fiber/coaxial (HFC) network is a scarce resource. The bandwidth itself is comparatively small (approximately 37 MHz as compared to the much greater bandwidth of approximately 814 MHz for the downstream band). The upstream band is shared by a plurality of cable modems and may be shared by other services, such as cable telephony, as well. Further, channel impairment such as ingress noise make burst transmission difficult.

Thus, the use of spectrum management according to the present invention facilitates the provisioning of radio frequency (RF) channels in a manner such that the RF channels are not impaired by ingress or the like and also are not utilized by other services. When channel impairments such as ingress noise do occur, the channel can be re-provisioned or moved to an unaffected radio frequency or channel.

According to the present invention, on-going channel monitoring, based upon the use of packet-based statistics and/or signal-to-noise ratio (SNR) and/or channel noise power is performed by the upstream receiver or cable modem termination system. By performing such monitoring at the cable modem termination system, spectrum analysis is provided at a single location and the need for an expensive, external spectrum management unit is eliminated.

Examples of the types of statistical information which may be utilized by the spectrum management/allocation circuit 15 to determine whether channel quality is sufficient to support 16-QAM, sufficient to support QPSK, or channel quality is insufficient to support either 16-QAM or QPSK and the channel must therefore be moved to a different spectral allocation, e.g., frequency band are provided below:

Statistics
Number of packets (total)
Number of packets undetected (no unique word)
Number of packets with corrected errors
Number of packets with uncorrectable errors
Number of FEC blocks (total)
Number of FEC blocks with corrected errors
Number of FEC blocks with uncorrectable errors

Referring now to FIG. 5, upstream channel quality information can also be used to facilitate the changing of physical layer parameters in real time. FIG. 5 shows Reed Solomon coding gain for various T's for 16-QAM where K=64 bytes. It is clear that as coding gain increases (increasing T), the probability of incurring a data transmission error P(e) decreases for any given signal-to-noise ratio.

The ability to change physical layer parameters in real time allows a given channel to be optimized when the channel quality is not low enough so as to cause either a change in modulation method or to necessitate that the channel be moved. Thus, according to the present invention, forward error correction (FEC) coding gain is increased and/or longer guard times are provided so as to facilitate reliable data transmission on such channels. Of course, it is understood that as the number of forward error correcting parity bytes is increased, coding gain is correspondingly increased for a given size of the information bytes.

Referring now to FIG. 6, the upstream transmitter of each cable modem and the burst receiver of the cable modem termination system utilize fine frequency agility so as to enhance the overall data throughput of the upstream band. Fine frequency agility includes both channel reallocation (so as to avoid channels having poor quality) and the definition of channels with a fine frequency resolution (so as to enhance the efficiency with which the frequency spectrum is divided among channels).

Thus, according to the present invention, fine frequency agility facilitates the definition of channels in the upstream band with a resolution of a few Hz. According to the present invention, upstream channels are characteristically defined in increments of about 1.0 Hz. Such fine tuning capability is particularly beneficial in the low frequency portion of the upstream band, where narrowband ingress is frequently present.

The use of such fine frequency agility facilitates the precise definition of upstream channels such that the usable upstream bandwidth is enhanced. That is, upstream channels can be defined such that the bandwidth of each upstream channel is as large as possible without including those portions of the upstream frequency spectrum which include narrowband interference. Thus, such fine tuning of the available spectrum mitigates waste due to unused, but otherwise good, i.e., not noisy, bandwidth proximate narrowband ingress. Such waste inherently results from the use of coarser spectrum division.

The ability to define upstream channels in this manner is substantially dependent upon the resolution with which the channels may be defined. Thus, the finer the resolution for defining the channels, the more readily such channels may be defined in a manner which optimizes the bandwidth (by mitigating waste of the available spectrum) thereof while still excluding undesirable narrowband interference.

Further, the carrier frequency may be fine tuned so as to avoid such interference in a non-uniform fashion. That is, each individual channel in the upstream band need not have the same bandwidth. Rather, non-uniform bandwidths may be utilized so as to tend to optimize the overall upstream data throughput.

It is important to note that the existing DOCSIS/IEEE specification only facilitates the allocation of upstream symbol rates (which are proportional to the upstream channel bandwidths)

according to powers-of-two. That is, each greater symbol rate is, according to DOCSIS/IEEE specifications, twice that of the preceding symbol rate. Thus, the DOCSIS/IEEE specifications do not facilitate enhancement of overall data throughput, as does the present invention. According to the present invention, symbol rates, e.g., bandwidths, may be varied in a nearly continuous manner, e.g., in 1.0 Hz increments. The ability to change symbol rates in such a near-continuous manner is a direct result of such fine frequency agility, wherein the bandwidth of each upstream channel can be defined to a resolution of a few Hz.

The ability to vary the upstream symbol rate according to other than powers of two is particularly important where multiple data rates, such as those frequently required by modem applications, are not themselves defined in powers of two.

Further, in the upstream band, where undesirable ingress in a channel frequently inhibits uniform channelization, being able to vary the data rate in a generally arbitrary manner allows data carrier frequencies to be positioned in between two narrowband interferences in a manner which tends to optimize the bandwidth thereof, so as to enhance overall data throughput of the upstream band.

An example of variable symbol rates between 100 kBaud to 5.12 Mbaud which are supported by the upstream channel is provided below:

Symbol Rate (kysm/sec.)	Channel Width (kHz, α=25%)	QPSK Date Rate (kbits/sec.)	16-QAM Date Rate (kbits/sec.)
128	160	256	512
160	200	320	640
256	320	512	1,024
320	400	640	1,280
512	640	1,024	2,048
640	800	1,280	2,560
1,024	1,280	2,048	4,096
1,280	1,600	2,560	5,120
2,048	2,560	4,096	8,192
2,560	3,200	5,120	10,240
4,096	5,120	8,192	16,384
5,120	6,400	10,240	20,480

As further shown in FIG. 6, a bad radio frequency (RF) channel 21 is moved to an unused channel 23 when the channel power, e.g., spectral density, of the bad channel exceeds a predetermined threshold level 24 or when any other monitored parameter indicates that channel quality is below a predetermined threshold. In this manner, channels are reallocated to locations having a higher quality and data throughput is enhanced.

The band to which such a channel is moved is the best channel available at that time. In this manner, channelization tends to utilize the best available channels and the data rates supported by each such best available channel tend to be maximized. Thus, the overall upstream data rate is substantially enhanced.

Alternatively, when a channel is moved away from a spectral location where the measured parameter which is indicative of channel quality indicates that the quality of the channel is below the predetermined threshold, then the new channel may be assigned by any desired method or even may be assigned arbitrarily, as long as the quality of the spectral location to which the channel is moved is above the predetermined threshold.

Referring now to FIG. 7, dynamic channel allocation control flow starts at block 30. The process continues for a predetermined evaluation time as shown by decision block 32, wherein a loop is incurred until the predetermined evaluation time has been exceeded. The evaluation time is that time during which upstream channels are monitored, so as to determine whether or not they are suitable for continued and/or future use. The evaluation time may be determined empirically.

During the evaluation time, if the number of undetected packets exceeds a predetermined threshold, as shown by decision block 34, then the signal-to-noise ratio is checked. If the signal-to-noise ratio is less than a predetermined threshold, then the symbol rate and constellation for a new, unused channel is determined as shown in block 44 and a channel reallocation message is sent to all cable modems in the frequency channel as shown in block 48.

If the signal-to-noise ratio is not less than the threshold, then the modulation for the upstream channel is changed to QPSK as shown in block 44.

Similarly, when the number of uncorrectable packets exceeds a predetermined threshold as shown in decision block 36, then the signal-to-noise ratio is compared to a predetermined threshold as shown in decision block 42 and symbol rate and constellation for a new upstream channel is determined as shown in block 44 when the signal-to-noise ratio is less than the predetermined threshold and the channel modulation method is changed to QPSK when the signal-to-noise ratio is not greater than the predetermined threshold, as shown in block 44.

When the signal-to-noise ratio is less than a predetermined threshold as shown in decision block 38, then the number of corrected packets is checked. When the signal-to-noise ratio is not greater than the predetermined threshold, then the process repeats. When the number of corrected packets is greater than a predetermined threshold as shown in decision block 40, then the signal-to-noise ratio is checked with respect to the predetermined threshold as shown in decision block 42. When the number of corrected packets is not greater the predetermined threshold, as shown in decision block 40, then the process repeats.

A spectrum analyzer 46 may be used to define the next available channel. The next available channel is that unused channel which is best suited for upstream communications. The local spectrum analyzer 46 may determine which unused channel is best suited for next use by looking at the signal, or the power thereof, which is present upon the used channel. Of course, that unused channel having the lowest signal or power is most likely best suited for use next.

Referring now to FIG. 8, CMTS dynamic channel allocation control flow is shown. Dynamic channel allocation starts 610, then waits 611 while two independent flow paths execute. According to the left flow path, a determination is made if the channel being monitored is bad, as shown in decision block 612. If the channel is not bad, then the process returns to the wait 611 state while right control path continues to execute. If the channel is bad, then the constellation is set to QPSK as shown in block 613 and ingress cancellation is applied on a per channel basis as shown in block 614. Intersymbol interference (ISI) mitigation is applied on a per user basis as shown in block 615.

If the noise-to-signal ratio is greater than a predetermined QPSK threshold, as indicated in decision block 616, then a final constellation is assigned as shown in block 622 and the left control path returns to the wait state 611.

If the noise-to-signal ratio is not greater than the QPSK threshold, then the next available channel is provided, if available, as shown in decision block 617 and block 21. If no next channel is available, then a new symbol rate is assigned as shown in block 619. The spectrum manager 618 controls this function.

As shown in the right control path, after the wait state 611 is entered, then each channel is checked on a per user base as shown in block 624. If each channel, on a per user base, is not found to be bad, then the wait state 611 is re-entered. If a channel is found to be bad on a per user basis, then ISI mitigation is employed on a per user basis as shown in block 623.

The channel quality evaluation criteria include the use of undetected packets as indicating a bad SNR, uncorrectable packets as indicating a marginal SNR and corrected packets as indicating an acceptable SNR. The equalizer acquisition time is configured such that ISI equalization is performed in less than 100 symbols and the ingress canceller is effective in 100 to 1,000 symbols.

It is understood that the exemplary method and apparatus described herein and shown in the drawings represents only presently illustrative embodiments of the invention. Indeed, various modifications and additions may be made to such embodiments without departing from the spirit and scope of the invention. For example, those skilled in the art will appreciate that various other measures of channel quality may be utilized for determining which modulation method is to be utilized upon a given channel and to determine whether or not the spectral allocation of the channel should be changed. For example, the reliability with which various different types of messages are received may be measured so as to provide such an indication of channel quality. Further, various different modulation methods, other than QPSK and 16-QAM, may be utilized. For example, the present invention may be utilized with 32-QAM, 64-QAM and 256-QAM. Thus, these and other modifications and additions may be obvious to those skilled in the art and may be implemented to adapt the present invention for use in a variety of different applications.

Cable Modem Termination System Upstream MAC/PHY Interface

The detailed description set forth below in connection with the appended drawings is intended as a description of an exemplary embodiment of the invention and is not intended to

represent the only form in which the present invention may be constructed or utilized. The detailed description sets forth the construction and functions of the invention, as well as the sequence of steps for operating the invention in connection with the illustrated embodiment. It is to be understood, however, that the same or equivalent functions may be accomplished by different embodiments that are also intended to be encompassed within the spirit and scope of the invention.

Referring now to FIG. 1, the present invention generally includes an interface between the physical layer burst receiver 11 and the MAC 13 of a cable modem termination system 8 which is in communication with a plurality of cable modems 9. The interface between the burst receiver 11 and the MAC 13 includes a data interface for communicating data from the burst receiver 11 to the MAC 13, an error information interface for communicating error information from the burst receiver 11 to the MAC 13 and a slot timing and data type interface for communicating information from the MAC 13 to the burst receiver 11, as described in detail below.

Prior to discussing the headend upstream MAC/PHY interface in detail, a robust technique for optimal upstream communications between a cable modem subscriber and a headend will be described in detail because it provides a helpful background for the description of the MAC/PHY interface.

According to one aspect, the present invention provides a technique in which a plurality of upstream channels are periodically monitored for at least one parameter which is indicative of channel quality. A first modulation method is used for each upstream channel for which the monitored parameter(s) indicate that channel quality is above a predetermined threshold value and a second modulation method is used for each upstream channel for which the monitored parameter(s) indicate that channel quality is below the predetermined threshold value. The first modulation method utilizes a larger constellation size than the second modulation method, such that a higher data rate is achieved when the channel quality is good enough to support the higher data rate.

Further, the present invention provides in another aspect a method and apparatus for optimizing the efficiency of upstream data communications by dividing an upstream spectrum into a plurality of upstream channels, wherein each upstream channel has a bandwidth of less than or equal to approximately 0.5 MHz. The upstream channels are periodically monitored for at least one parameter which is indicative of the quality of each monitored upstream channel. Communications are moved from a used channel an unused channel when the monitored parameter(s) indicate that the quality of the used channel is below a predetermined threshold. In this manner, noisy channels tend to be avoided and communications occur on higher quality channels which are capable of supporting higher data rates.

The present invention in another aspect provides a method and apparatus for tending to optimize upstream communication efficiency wherein a communications channel having upper and lower frequency bounds is defined in an attempt to determine an optimal bandwidth of the channel given constraints imposed by the presence of adjacent channels, as well as constraints imposed by narrowband interference. Data rate is thus enhanced by varying the symbol rate of

communications performed via the channel in a near-continuous manner, i.e., by varying the upper and/or lower frequency bounds, so as to enhance the bandwidth and thereby enhance the efficiency with which the available frequency spectrum is utilized.

Thus, according to the present invention, the data rate of the upstream channel tends to be optimized, so as to enhance the data communication efficiency of the upstream channel.

The present invention provides enhanced upstream data rates by utilizing a constellation which is efficient in view of transmission medium conditions, by providing fine frequency agility based upon channel quality monitoring so as to enhance the effectiveness with which the limited bandwidth of the upstream channel is utilized, and by providing nearly continuous symbol rate switching so as to facilitate the usage of an enhanced symbol rate which is compatible with line conditions.

Referring now to FIG. 2, according to contemporary practice a cable modem termination system includes a plurality of demodulators 10A-10Z which receive modulated data which is input from a plurality of cable modems via a common transmission medium. The demodulators 10A-10Z provide a demodulated data output for the frequency division multiplexed (FDM) upstream channels via which data is transmitted from the plurality of cable modems to the cable modem termination system (CMTS). The cable modems communicate with the cable modem termination system via time division multiple access (TDMA), wherein a plurality of cable modems communicate with each demodulator 10A-10Z and wherein the cable modems associated with each demodulator 10A-10Z are distinguished from those associated with a different demodulator via frequency division multiplexing (FDM).

Referring now to FIG. 3, according to the present invention monitoring circuit 12 of the cable modem system 36 monitors the ability of each FDM channel to reliably transmit data at a desired data rate. That is, a parameter which is indicative of channel quality is periodically monitored so as to determine the ability of the channel to facilitate upstream data communications. The channel monitoring function is, for example, incorporated into each individual burst receiver, of which there are typically eight per cable modem termination system. The averaging and statistic gathering function is may be common to all channels, and thus may reside separate from the individual burst receivers.

As used herein, channel quality is defined as the ability of a channel to transmit data reliably thereon, such that higher quality channels transmit data reliably at a higher data rate than lower quality channels.

When a quality of the channel, such as signal-to-noise (SNR) is determined to be above a predetermined threshold value, then a first modulation method is utilized for that upstream channel. When the quality of a channel is determined to be less than that of the predetermined threshold value, then a second modulation method is utilized. The first modulation method is capable of providing a higher data rate than the second modulation method. According to the illustrated embodiment of the present invention, first modulation method has a larger constellation size than the second modulation method. According to the exemplary embodiment of the present invention, the first modulation method encompasses 16-QAM and the second modulation method encompasses QPSK (4-QAM). Thus, according to the present invention, a

constellation size is selected which is dependent upon transmission medium characteristics, such that the data rate of communications on each channel tends to be enhanced.

Alternatively, more than two different modulation methods may be utilized. Thus, a plurality of different modulation methods, wherein each individual modulation method is generally better suited for a different range of channel quality, may be utilized. In this manner, the efficiency of data communications is yet further enhanced.

The modulation method utilized for each upstream channel is communicated from the monitoring circuit 12 to each demodulator 14a-14z of the cable modem termination system and is also inserted into the downstream message flow such that the modulation method is communicated to each cable modem 30, thereby facilitating modulation by each cable modem with the desired modulation method.

Thus, each cable modem 30 includes a demodulator 32 for demodulating downstream data transmissions from the cable modem termination system 36 and also includes a modulator 34 for modulating upstream data transmissions. A central circuit 38 of the cable mode 30 controls the modulation method utilized by the modulator 34 and also controls the physical layer parameters such as forward error correcting gain and guard time.

According to one exemplary embodiment of the present invention, the step of periodically monitoring a plurality of channels contemplates periodically monitoring a signal-to-noise ratio for each of the monitored channels. The signal-to-noise ratios are monitored over a plurality of separate communications bursts and an average of the signal-to-noise ratios is formed from the individual measurements. This average is compared to the predetermined threshold value so as to determine whether or not a change is to be made to the modulation method.

In an exemplary aspect of the invention, the predetermined signal-to-noise ratio threshold value is approximately 20 dB. Thus, if the signal-to-noise ratio is equal to or greater than 20 dB, then the first modulation method is utilized and when the signal-to-noise ratio is less than 20 dB, then the second modulation method is utilized.

In particular, the monitoring circuit 12 defines a portion of the cable modem termination system. Alternatively, the monitoring circuit 12 may be separate from the cable modem termination system, but might be located generally proximate thereto, such that an accurate assessment of each channel's ability to transmit data may be performed.

According to another exemplary embodiment of the present invention, the step of periodically monitoring a plurality of channels contemplates periodically monitoring channel noise power. Thus, channel noise power may be monitored and compared to a predetermined threshold value so as to determine which modulation method is to be utilized. Channel noise may be monitored in addition to signal-to-noise ratio (SNR) and/or any other desired parameter which is indicative of channel quality, such as channel statistics. Thus, any desired combination of parameters indicative of channel quality may be utilized according to the method of the present invention.

According to yet another exemplary embodiment of the present invention, the step of periodically monitoring a plurality of channels contemplates periodically monitoring channel statistics for each of the monitored upstream channels. Examples of the statistics which may be

monitored for each upstream channel include the number of packets undetected, the number of packets with corrected errors, the number of packets with uncorrected errors, the number of forward error correction blocks with corrected errors, and the number of forward error correction blocks with uncorrected errors. Combinations of these criteria and/or other desired criteria may similarly be monitored. Thus, it will be appreciated that such channel statistics provide an indication of the quality of an upstream channel which may be utilized to determine which modulation method may be utilized to reliably and efficiently transmit data upon that channel.

Optionally, at least one physical layer parameter of a channel may be changed in response to a change in quality of the channel. For example, forward error correcting gain and/or the guard time associated with a channel may be changed in response to a change in the quality of the channel. This change in the physical layer parameter may be either in addition to or separate from any change in modulation methods.

Although periodic monitoring of one or more parameters indicative of channel quality is performed according to the exemplary embodiment of the present invention, those skilled in the art will appreciate that continuous monitoring at such parameters may alternatively be utilized, if desired.

It is important to note that the individual channel demodulators 14a-14z collect data, while the monitoring circuit 12 averages the data collected on each 14a-14z, so as to provide the statistics necessary for the monitoring circuit to control the individual channel demodulators 14a-14z.

Referring now to FIG. 4, a prior art method for receiving modulated data at a cable modem termination system from a transmission medium, such as a coaxial cable, and for converting that received modulated data into digital data suitable for computer use includes demodulating the modulated data via an upstream burst receiver 11 and providing the demodulated data to medium access control (MAC) 13. Medium access control (MAC) 13 controls access of the cable modem termination system to the transmission medium and provides a digital data output representative of a message transmitted from a cable modem.

The upstream burst receiver is configured so as to be capable of demodulating both QPSK and 16-QAM modulation formats within a TDMA frame. According to contemporary methodology, the upstream burst receiver 11 is configured so as to demodulate modulated data from the transmission medium according to a single, predetermined modulation method. The predetermined modulation method must be selected such that it provides reliable data transmission for a wide range of transmission medium conditions. Of course, this necessitates that a modulation technique which provides reliable data transmission even under the worst expected transmission medium conditions must be utilized. As those skilled in the art will appreciate, such a modulation technique, QPSK for example, does not provide the enhanced data rates which may be possible when better medium conditions are present. That is, when only a single modulation method is utilized, then data rate must typically be sacrificed in order to provide the desired reliability.

Thus, in order to limit interruptions to upstream communications, cable modem systems typically utilize an upstream modulation method which is compatible with the lowest expected channel quality. However, as those skilled in the art will appreciate, such worst case modulation methods (QPSK, for example) are inherently inefficient at higher channel qualities. The modulation methods used for lower channel qualities provide reduced bit rates, while the modulation methodology suitable for higher channel qualities provide higher bit rates.

It is important to recognize that upstream data communications are characterized by a plurality of different time division multiplexed channels, wherein each individual channel originates from a different cable modem or a different group of cable modems. Because the transmission path between the cable modem termination system and each individual cable modem is not identical (even though a common coaxial cable may be utilized along some portion of the path), variations in channel quality occur. Thus, a wide variation in channel quality among channels, i.e., cable modems, is typical. These variations may occur because, for example, some of the cable modems and/or their links to the common coaxial cable are located proximate noise sources.

Referring now to FIG. 4, according to the present invention the cable modem termination system includes a spectrum management/allocation circuit 15 (as also shown in FIG. 2) which at least periodically monitors the plurality of upstream channels for at least one parameter which is indicative of channel quality. For example, spectrum management/allocation circuit 15 may receive signal-to-noise ratio or channel power values from the upstream burst receiver 11. Alternatively, the spectrum management/allocation circuit 15 receives packet/FEC status from a upstream MAC/PHY channel statistics circuit 12. The upstream MAC/PHY channel statistics circuit receives the output of the upstream burst receiver prior to the output of the upstream burst receiver being provided to the medium access control 13 and the upstream MAC/PHY channel statistic circuit 12 calculates the packet/FEC statistics, which is then provided to spectrum management/allocation circuit 15.

Any desired combination of signal-to-noise ratio, channel power, packet statistics and/or forward error correction statistics may be utilized as the parameter which is indicative of channel quality.

Such monitoring of the signal-to-noise (SNR), channel power, and/or packet/FEC statistics facilitates the determination of which modulation method, e.g., QPSK or 16-QAM, is to be utilized as long as the quality of the channel is deemed to be sufficiently good to facilitate the use of such modulation methods. When the quality of the channel is insufficient to facilitate the use of the smallest constellation size, i.e., QPSK, then the spectral allocation of the channel is changed, as discussed in detail below.

Optional averaging circuit 17 averages a plurality of signal-to-noise (SNR) or channel power measurements to compensate for short term fluctuations therein.

When a change in modulation method is indicated, then the new modulation method is transmitted from a switch circuit 16 of the spectrum management/allocation circuit 15 to the upstream burst receiver 11 and is also transmitted to the affected cable modem via downstream message flow, as mentioned above.

When the quality of a channel is determined to be sufficiently poor (such that even QPSK will not provide reliable data transmission), then that channel may be moved to a different frequency allocation. When this occurs, the new upstream channel frequency is transmitted to the upstream burst receiver 11 and is also transmitted to the affected cable modem via downstream message flow.

A bandwidth selection circuit 19 of the spectrum management/allocation circuitry 15 thus facilitates the implementation of fine frequency agility and the switch 16. The bandwidth selection circuit 19 determines the bandwidth of each downstream channel and the switch 16 effects switching to the desired channel by the burst receiver 11. The upstream spectrum is divided into a plurality of upstream channels and wherein each channel is characterized as having a bandwidth which is less than or equal to 0.5 MHz.

According to the fine frequency agility aspect of the present invention, the spectrum management/allocation circuit 15 monitors the upstream channels for at least one parameter which is indicative of the quality of each monitored upstream channel and moves communications from a used channel to an unused channel when the monitored parameter indicates that the quality of the used channel is below a predetermined threshold value.

Thus, according to the present invention, 16-QAM is the baseline or default modulation method and QPSK is the fall-back modulation method, which is utilized only when channel quality is insufficient to support upstream data transmission utilizing 16-QAM. Channel reallocation is the fall-back method used when channel quality is insufficient for the use of QPSK.

The use of 16-QAM enhances channel band with efficiency by a factor of 2, typically from approximately 1.6 bits/Hz to approximately 3.2 bits/Hz, while providing approximately 25 percent excess bandwidth. For example, the use of 16-QAM provides up to 20.48 Mbps at 5.12 Mbaud.

However, it is important to appreciate that the detection of 16-QAM is much more difficult than the detection of QPSK, since the demodulation is amplitude sensitive, as well as phase sensitive when utilizing 16-QAM, whereas demodulation is only phase sensitive when utilizing QPSK.

It is expected that the above discussed combination of variable constellation size and fine frequency agility, i.e., dynamic channel allocation, will enhance channel bandwidth efficiency substantially.

It is important to understand that the upstream bandwidth in a hybrid fiber/coaxial (HFC) network is a scarce resource. The bandwidth itself is comparatively small (approximately 37 MHz as compared to the much greater bandwidth of approximately 814 MHz for the downstream band). The upstream band is shared by a plurality of cable modems and may be shared by other services, such as cable telephony, as well. Further, channel impairment such as ingress noise make burst transmission difficult.

Thus, the use of spectrum management according to the present invention facilitates the provisioning of radio frequency (RF) channels in a manner such that the RF channels are not impaired by ingress or the like and also are not utilized by other services. When channel

impairments such as ingress noise do occur, the channel can be re-provisioned or moved to an unaffected radio frequency or channel.

According to the present invention, on-going channel monitoring, based upon the use of packet-based statistics and/or signal-to-noise ratio (SNR) and/or channel noise power is performed by the upstream receiver or cable modem termination system. By performing such monitoring at the cable modem termination system, spectrum analysis is provided at a single location and the need for an expensive, external spectrum management unit is eliminated.

Examples of the types of statistical information which may be utilized by the spectrum management/allocation circuit 15 to determine whether channel quality is sufficient to support 16-QAM, sufficient to support QPSK, or channel quality is insufficient to support either 16-QAM or QPSK and the channel must therefore be moved to a different spectral allocation, e.g., frequency band are provided below:

Statistics
Number of packets (total)
Number of packets undetected (no unique word)
Number of packets with corrected errors
Number of packets with uncorrectable errors
Number of FEC blocks (total)
Number of FEC blocks with corrected errors
Number of FEC blocks with uncorrectable errors

Referring now to FIG. 5, upstream channel quality information can also be used to facilitate the changing of physical layer parameters in real time. FIG. 5 shows Reed Solomon coding gain for various T's for 16-QAM where K=64 bytes. It is clear that as coding gain increases (increasing T), the probability of incurring a data transmission error P(e) decreases for any given signal-to-noise ratio.

The ability to change physical layer parameters in real time allows a given channel to be optimized when the channel quality is not low enough so as to cause either a change in modulation method or to necessitate that the channel be moved. Thus, according to the present invention, forward error correction (FEC) coding gain is increased and/or longer guard times are provided so as to facilitate reliable data transmission on such channels. Of course, it is understood that as the number of forward error correcting parity bytes is increased, coding gain is correspondingly increased for a given size of the information bytes.

Referring now to FIG. 6, the upstream transmitter of each cable modem and the burst receiver of the cable modem termination system utilize fine frequency agility so as to enhance the overall data throughput of the upstream band. Fine frequency agility includes both channel reallocation (so as to avoid channels having poor quality) and the definition of channels with a fine frequency resolution (so as to enhance the efficiency with which the frequency spectrum is divided among channels).

Thus, according to the present invention, fine frequency agility facilitates the definition of channels in the upstream band with a resolution of a few Hz. According to the present invention, upstream channels are characteristically defined in increments of about 1.0 Hz. Such fine tuning capability is particularly beneficial in the low frequency portion of the upstream band, where narrowband ingress is frequently present.

The use of such fine frequency agility facilitates the precise definition of upstream channels such that the usable upstream bandwidth is enhanced. That is, upstream channels can be defined such that the bandwidth of each upstream channel is as large as possible without including those portions of the upstream frequency spectrum which include narrowband interference. Thus, such fine tuning of the available spectrum mitigates waste due to unused, but otherwise good, i.e., not noisy, bandwidth proximate narrowband ingress. Such waste inherently results from the use of coarser spectrum division.

The ability to define upstream channels in this manner is substantially dependent upon the resolution with which the channels may be defined. Thus, the finer the resolution for defining the channels, the more readily such channels may be defined in a manner which optimizes the bandwidth (by mitigating waste of the available spectrum) thereof while still excluding undesirable narrowband interference.

Further, the carrier frequency may be fine tuned so as to avoid such interference in a non-uniform fashion. That is, each individual channel in the upstream band need not have the same bandwidth. Rather, non-uniform bandwidths may be utilized so as to tend to optimize the overall upstream data throughput.

It is important to note that the existing DOCSIS/IEEE specification only facilitates the allocation of upstream symbol rates (which are proportional to the upstream channel bandwidths) according to powers-of-two. That is, each greater symbol rate is, according to DOCSIS/IEEE specifications, twice that of the preceding symbol rate. Thus, the DOCSIS/IEEE specifications do not facilitate enhancement of overall data throughput, as does the present invention. According to the present invention, symbol rates, e.g., bandwidths, may be varied in a nearly continuous manner, e.g., in 1.0 Hz increments. The ability to change symbol rates in such a near-continuous manner is a direct result of such fine frequency agility, wherein the bandwidth of each upstream channel can be defined to a resolution of a few Hz.

The ability to vary the upstream symbol rate according to other than powers of two is particularly important where multiple data rates, such as those frequently required by modem applications, are not themselves defined in powers of two.

Further, in the upstream band, where undesirable ingress in a channel frequently inhibits uniform channelization, being able to vary the data rate in a generally arbitrary manner allows data carrier frequencies to be positioned in between two narrowband interferences in a manner which tends to optimize the bandwidth thereof, so as to enhance overall data throughput of the upstream band.

An example of variable symbol rates between 100 kBaud to 5.12 Mbaud which are supported by the upstream channel is provided below:

Symbol Rate (kysm/sec.)	Channel Width (kHz, α=25%)	QPSK Date Rate (kbits/sec.)	16-QAM Date Rate (kbits/sec.)
128	160	256	512
160	200	320	640
256	320	512	1,024
320	400	640	1,280
512	640	1,024	2,048
640	800	1,280	2,560
1,024	1,280	2,048	4,096
1,280	1,600	2,560	5,120
2,048	2,560	4,096	8,192
2,560	3,200	5,120	10,240
4,096	5,120	8,192	16,384
5,120	6,400	10,240	20,480

As further shown in FIG. 6, a bad radio frequency (RF) channel 21 is moved to an unused channel 23 when the channel power, e.g., spectral density, of the bad channel exceeds a predetermined threshold level 24 or when any other monitored parameter indicates that channel quality is below a predetermined threshold. In this manner, channels are reallocated to locations having a higher quality and data throughput is enhanced.

The band to which such a channel is moved is the best channel available at that time. In this manner, channelization tends to utilize the best available channels and the data rates supported by each such best available channel tend to be maximized. Thus, the overall upstream data rate is substantially enhanced.

Alternatively, when a channel is moved away from a spectral location where the measured parameter which is indicative of channel quality indicates that the quality of the channel is below the predetermined threshold, then the new channel may be assigned by any desired method or even may be assigned arbitrarily, as long as the quality of the spectral location to which the channel is moved is above the predetermined threshold.

Those skilled in the art will appreciate that various other measures of channel quality may be utilized for determining which modulation method is to be utilized upon a given channel and to determine whether or not the spectral allocation of the channel should be changed. For example, the reliability with which various different types of messages are received may be measured so as to provide such an indication of channel quality. Further, various different modulation methods, other than QPSK and 16-QAM, may be utilized.

After the ranging process has been performed so as to adjust the power level of at least one cable modem so as to normalize the power of a received transmission at the cable modem termination system, adjust the carrier frequency of the cable modem so as to enhance

channelization in the frequency domain, and adjust slot timing of a transmission from the cable modem so as to compensate for propagation delays, data packets transmitted from the cable modem to the cable modem termination system may be acquired by the cable modem termination system.

As those skilled in the art will appreciate, contemporary cable modem termination systems include a burst receiver, a continuous transmitter and a medium access control (MAC) for controlling access of an external device, such as a computer, network, or other data serving device to the physical layer of the cable modem termination system.

In a contemporary cable modem termination system, the burst receiver merely communicates demodulated received data packets to the medium access control, which forwards the received data packets to an external device. Further communications occur between the burst receiver and the medium access control which enhance communications between a cable modem and the cable modem termination system.

More particularly, information is communicated from the MAC to the burst receiver which is representative of parameters of received time division multiple access data. According to one aspect of the present invention, the information representative of parameters of the received time division multiple access data is used by the burst receiver to facilitate processing of the received time division multiple access signal, as described in detail below.

According to another aspect of the present invention, time division multiple access communications are enhanced by communicating information from the burst receiver to the MAC. The information is representative of error conditions related to an upstream channel, as described in detail below.

More particularly, slot timing information and/or data-type information is communicated from the MAC to the burst receiver to facilitate processing of upstream data packets by the burst receiver. The slot timing information include information representative of a start time and a stop time of time division multiple access time slots. Thus, the slot timing information may include either start time and stop time, start time and duration or stop time and duration.

The slot timing and data-type information for each slot include a station or service identifier (SID) value which identifies a transmitter, e.g., cable modem, which is transmitting a data packet within the slot, the time at which the slot began and an interval usage code which defines a burst type of the data packet transmitted within the slot.

The data-type information include information representative of a QPSK/QAM modulation type which was used to modulate the upstream data packets. For example, the data-type information identifies the upstream data packet as being modulated by QPSK or 16-QAM.

As mentioned above, the communication of slot timing information and/or data-type information is performed after a ranging process, such that the power level, carrier frequency and slot timing of the received upstream data packets have been adjusted to desirable values.

According to the other aspect of the present invention, error information is communicated from the burst receiver to the MAC to estimate the channel quality. Thus, the error information facilitates spectrum allocation or channel assignments and also facilitates the making of

adjustments to forward error correction gain in upstream data transmissions. Also, the communicated error information facilitates changes in guard band widths in upstream data transmissions.

The error information communicated from the burst receiver to the MAC is representative of forward error correction errors and/or packet error statistics. Information is, for example, transmitted from the burst receiver to the MAC as a series of data bursts. Error information is also, for example, transmitted from the burst receiver to the MAC as a series of data bursts. The data bursts for both the data and the error information may be, for example, transmitted at a serial clock rate of the burst receiver.

According to one exemplary embodiment of the present invention, the error information is transmitted from the burst receiver to the MAC as prepend information. Thus, the present invention optionally includes the prepending of control information to data which is sent from the burst receiver to the MAC. The prepended control information include channel statistics.

The channel statistics of the prepended information include, for example, FECOK, correctable FEC error, uncorrected FEC error, no unique word detected, collided packet, no energy, and packet length violation.

The MAC may determine additional statistics from the prepended channel statistics. Such additional statistics include, for example, number of slots, number of slots with power but no data, number of slots with bad data, number of good data slots, total number of FEC blocks, number of FEC blocks with correctable errors, number of uncorrectable FEC blocks, number of requests received, number of collided requests, number of corrupted requests, number of packets received, number of collided packets, number of corrupted packets, number of ranging messages received, number of collided ranging messages received and number of corrupted ranging messages.

Referring now to FIG. 7A, a sample data packet 50 includes a QPSK-like portion 56 and a QPSK or 16-QAM 57 payload 54. Guard times 55 are typically used between adjacent data packets.

The QPSK or QPSK-like portion 56 includes a preamble 51 which contains a unique word 52, and, optionally, an equalization training 53 or ranging portion which facilitates ranging, as described in detail above.

Referring now to FIG. 8, dynamic channel allocation control flow starts at block 30. The process continues for a predetermined evaluation time as shown by decision block 32, wherein a loop is incurred until the predetermined evaluation time has been exceeded. The evaluation time is that time during which upstream channels are monitored, so as to determine whether or not they are suitable for continued and/or future use. The evaluation time may be determined empirically.

During the evaluation time, if the number of undetected packets exceeds a predetermined threshold, as shown by decision block 34, then the noise-to-signal ratio is checked. If the noise-to-signal ratio is less than a predetermined threshold, then the symbol rate and constellation for a new, unused channel is determined as shown in block 44 and a channel reallocation message is sent to all cable modems in the frequency channel as shown in block 48.

If the noise-to-signal ratio is not less than the threshold, then the modulation for the upstream channel is changed to QPSK as shown in block 44.

Similarly, when the number of uncorrectable packets exceeds a predetermined threshold as shown in decision block 36, the noise-to-signal ratio, then the noise-to-signal ratio is compared to a predetermined threshold as shown in decision block 42 and symbol rate and constellation for a new upstream channel is determined as shown in block 44 when the noise-to-signal ratio is less than the predetermined threshold and the channel modulation method is changed to QPSK when the noise-to-signal ratio is not less than the predetermined threshold, as shown in block 44.

When the noise-to-signal ratio is less than a predetermined threshold as shown in decision block 38, then the number of corrected packets is checked. When the noise-to-signal ratio is not greater than the predetermined threshold, then the process repeats. When the number of corrected packets is greater than a predetermined threshold as shown in decision block 40, then the noise-to-signal ratio is checked with respect to the predetermined threshold as shown in decision block 42. When the number of corrected packets is not greater the predetermined threshold, as shown in decision block 40, then the process repeats.

A spectrum analyzer 46 may be used to define the next available channel. The next available channel is that unused channel which is best suited for upstream communications. The local spectrum analyzer 46 may determine which unused channel is best suited for next use by looking at the signal, or the power thereof, which is present upon the used channel. Of course, that unused channel having the lowest signal or power is most likely best suited for use next.

It is understood that the exemplary method and apparatus described herein and shown in the drawings represents only presently illustrative embodiments of the invention. Indeed, various modifications and additions may be made to such embodiments without departing from the spirit and scope of the invention. For example, those skilled in the art will appreciate that various other measures of channel quality may be utilized for determining which modulation method is to be utilized upon a given channel and to determine whether or not the spectral allocation of the channel should be changed. For example, the reliability with which various different types of messages are received may be measured so as to provide such an indication of channel quality. Further, various different modulation methods, other than QPSK and 16-QAM, may be utilized. Thus, these and other modifications and additions may be obvious to those skilled in the art and may be implemented to adapt the present invention for use in a variety of different applications.

Referring now to FIG. 9, the upstream minislot and interval definition is shown. According to one example of the present invention, a minislot clock (MSCLK) defines a plurality of minislots 101, wherein each new minislot occurs at the rising edge 102 of the minislot clock 100. A plurality of minislots typically define each of the request interval 104, the maintenance interval 105, and the data interval 106 of a MAP 107.

The request interval 104 of the MAP 107 defines a time period during which the plurality of cable modems may contend for the transmission of a request to the cable modem termination system. The request is a request to send a specified amount of data from the cable modem to the cable modem termination system.

The maintenance interval 105 of the MAP 107 is used to facilitate housekeeping functions such as ranging, as discussed in detail above. The data interval 106 of the MAP 107 defines the time slot within which data is transferred from a particular cable modem to the cable modem termination system. It is information about this data interval 106 which is communicated from the MAC to the burst receiver according to one aspect of the present invention. This data includes information representative of the start time and the duration of the data interval 106. By communicating information representative of the start time and duration of the data interval 106 from the MAC to the burst receiver, the burst receiver is able to process incoming data packets more efficiently. Since the burst receiver when to expect data packets from individual cable modems, the burst receiver is able to easily separate the data packets from different cable modems from one another and to perform subsequent processing thereupon.

Many of the terms and abbreviations discussed below are explained and/or defined in the Data-Over-Cable Service Interface Specifications (DOCSIS) Radio Frequency Interface Specification SP-RFI-I02-971008, which is the Multimedia Cable Network System (MCNS) specification for cable modem systems, the contents of which are hereby incorporated by reference.

Referring now to FIG. 10, the MAP message 110 format prior to processing by the message filter of the MAC is shown. The MAP message 110 typically contains a MAC management header 111 which contains information which facilitates desired processing by the MAC. An upstream channel ID 112 indicates which upstream frequency channel the MAP message is to be applied to. The UCD count 113 matches the value of the configuration change count of the UCD which describes the burst parameters which apply to the MAP.

The number of elements 114 provides an indication of the number of elements transmitted in this map. The allocation start time 116 indicates the effective start time from cable modem termination system initialization (in units of minislots) available for assignments according to this MAP. The acknowledgment (Ack) 118 indicates the latest time, from cable modem termination system initialization (in units of minislots) which has been processed in the upstream data communications. This time is used by the cable modems for collision detection purposes.

The ranging back-off start 119 is an initial back-off window for initial ranging contention, expressed as a power of two. Values for the ranging back-off start range from 0 to 15, wherein the highest order bits must be unused and set to 0.

The ranging back-off end 120 is the final back-off window for initial ranging contention, expresses a power of two. Values for the ranging back-off end 120 range from 0 to 15, wherein the highest order bits must be unused and set to 0.

MAP information elements 123 define the time slots during which individual cable modems transmit on a particular upstream channel to the cable modem termination system. A plurality of intervals of the MAP, such as the first interval 125, the second interval 126, and the last interval 127, define the individual time slots.

Each interval 125-127 includes a station or service identifier (SID) value 130 which identifies the cable modem for which the interval (and therefore the time slot defined thereby, applies. SID equals 0 defines the end of the list of intervals, thus indicating that all intervals have

been defined. The interval usage code (IUC) 131 defines the burst parameters to be utilized during the specified timing slot. Such burst parameters include the modulation type, e.g., QPSK or 16-QAM. The offset 132 indicates when, with respect to a common time reference, each interval begins. Offset equals 0 defines a beginning of the first interval.

Optionally, each MAP has a fixed length and format, such that unused intervals 140 may occur after the last interval 127. Acknowledgment and deferrals 141 optionally may be inserted into the list of intervals, generally after the end of list 128.

Referring now to FIG. 11, after the format of the MAP message has been filtered by the MAC for communication from the MAC to the burst receiver, the MAP message include an allocation start time 150 and a plurality of MAP information elements 151-153. Each MAP information element generally includes a service ID 155 which identifies the cable modem for which the slot time of the MAP information applies, an interval usage code 156 which identifies the burst type utilized by the cable modem during the time slot, and also identifies the slot time, typically in units of minislots.

Referring now to FIG. 12, the architecture of an exemplary shared SRAM-based MAP interface of a MAC for eight upstream channels of an exemplary cable modem termination system is shown. A MAP message filter 160 receives downstream MAC frames which contain MAPs having the message format shown in FIG. 10, as it is constructed prior to filtering. The MAP message filter 160 filters each MAP message so as to provide a filtered MAP message having a format such as that shown in FIG. 11.

After filtering, the contents of the filtered MAP are stored in 64x9 MAP internal FIFO 161 and the channel to which the MAP message applies is stored in 16x8 channel select FIFO 162. SRAM controller 163 then controls the storage of the MAP internal FIFO 161 contents and the channel select FIFO 162 contents in an external 64Kx16 SRAM 164 and then the SRAM controller 163 effects the transmission of the contents of the external 64Kx16 SRAM 164 to the appropriate, e.g., proper channel, MAP control interface 165-167.

Each MAP control interface 165-167 provides control signals from the MAC to one of eight burst receivers of the cable modem termination system. The control signals include minislot clock (MSCLK), Map Valid (MapValid), Map Clock (MapClk)and Map Data (MapData).

Instead of having an offset field which is defined in the original DOCSIS specification, two adjacent offsets are subtracted so as to compute the actual length of the interval in units of minislots.

Referring now to FIG. 13, the interface between each MAP control interface 165-167 (shown in FIG. 12) includes four conductors which provide communication from the MAP control interface to the burst receiver demodulator 170. It is important to appreciate that generally there is a dedicated MAP control interface 165-167 for each of eight burst receiver demodulators 170. Thus, there is a dedicated pair of MAP control interfaces 165-167 and burst receiver demodulators 170 for each upstream frequency channel.

Thus, FIG. 13 shows the signals for one channel of the MAP control interface between the MAC and the burst demodulator. There are a total of four signals MSCLK, MapValid,

MapData, MapClk, and each of these four signals are replicated for each upstream channel. MSLK provides the burst demodulator with a timing reference for minislots. According to the present invention, each rising edge of the MSLK signal defines the beginning of an upstream minislot. The MapValid, MapData and MapClk form a serial interface which transfers the 32 bit MAP information element stored in memory to the demodulator of the burst receiver at the appropriate time.

As shown in FIGs. 12 and 13, minislot clock (MSCLK), Map Valid (MapValid), Map Data (MapData) and Map Clock (MapClk) signals are communicated from each MAP control interface 165-167 to each demodulator 170.

Referring now to FIG. 14, timing control of the MAP which defines the upstream request interval 104, maintenance interval 105 and data interval 106 (as shown in FIG. 9) is shown.

The minislot count 180 begins at the beginning of the request interval 104 and continues until the end of the data interval 106. The minislot clock 100 provides for the timing of the request interval 104, maintenance interval 105 and data interval 106 as discussed above. A Map Valid signal 190 transitions to a low state 191 when Map Valid data 200 is present.

Map Data 200 may, for example, contain 32 bits of data which define a station or service identifier (SID) 155 (14 bits) which identifies the cable modem which is providing the upstream communication, an interval usage code 156 (4 bits)which defines the modulation type utilized by the cable modem, and a region length and minislots 157 (14 bits) which defines the length of the time slot which contains the data being transmitted from the cable modem to the cable modem termination system.

A Map Clock 210, typically running at a much higher rate than the minislot clock 100, defines the timing of the station or service identifier (SID) 155, the interval usage code 156 and the region length and minislots 157.

The MAP control interface of the MAC derives the starting time for each MAP interval from the allocation start time and the length of the previous MAP interval. The MAP control interface of the MAC transfers the MAP information element (IE) when its internal minislot count is less than one starting time of the MAP interval. A MAP information element (IE) is transferred, as shown by the MapValid signal going low, after the minislot count turns to N+2, and the starting time of the MAP interval for the information element (IE) being transferred is minislot N+3. For the burst demodulator, the rising edge of the minislot clock (MSCLK) signal right after a rising edge of the MapValid signal defines the beginning of the MAP interval for the MAP information element (IE) just received.

The time critical MAP interface includes two important concepts. First, the processing of the MAP message and conversion to a simplified format which is acceptable to the PHY or demodulator of the burst receiver, second, the use of a set of control signals to communicate this MAP information to the demodulator of the burst receiver utilizing a 4-signal interface.

Referring now to FIG. 15, inference of the receive now (Rx_now) 220 signal for a maintenance interval 105, having a length of 6 minislots, for example, is shown. The Receive now 220 signal is provided at the beginning of a minislot 220 which is the first minislot of the

maintenance interval (as shown in FIG. 15) and provides an indication that the maintenance interval has begun.

For maintenance intervals, including initial and station maintenance, and data intervals, including both short and long data intervals, the burst demodulator is configured to receive only one packet per interval. Thus, the beginning of the MAP interval represents the Receive_now signal for the burst demodulator.

Referring now to FIG. 16, in a similar manner, a Receive_now 220 signal is inferred for a data interval 106 and is issued at the beginning of the first minislot of the data interval 106.

Referring now to FIG. 17, a plurality of Receive_now signals 220 may be associated with each request interval, since each request interval may contain a plurality of requests, each request from a different cable modem.

The multimedia cable network system (MCNS) Data-Over-Cable Service Interface Specifications (DOCSIS) radio frequency interface specification (SP-RFI-I02-971008) protocol specifies a time-division multiple access (TDMA) protocol for the upstream transmission of data packets from cable modems to a cable modem termination system. In order to send data upstream, each cable modem must request a data slot large enough to hold the desired data. The CMTS responds to such request from the cable modems with a logical message (MAP) which is broadcast to all of the cable modems on a particular frequency channel. The MAP message specifies the upstream framing structure, so as to provide individual time slots within which each cable modem may transmit. The MAP specifies which cable modems may transmit, when they may transmit, and how, e.g., using what modulation type, they may utilize to transmit. When the appropriate TDMA time slot arrives (in time) a cable modem sends a burst of data, e.g., a data packet, to the cable modem termination system.

Each cable modem is typically identified by one or more station or service identifier (SID). Each TDMA time slot is typically an integer number of minislots, wherein each minislot is an arbitrary timing reference provided by the medium access control (MAC). The MCNS protocol negotiates sets of transmission parameters between the cable modems and the cable modem termination system. The parameters define how data is formatted during upstream bursts from each cable modem to the cable modem termination system. The DOCSIS protocol currently defines six burst types which may be used in upstream communications. Each burst type defines the modulation to be utilized during such upstream communications. The burst type is constant during a particular window in time, e.g., a time slot, and the burst type is designated by an interval usage code (IUC).

The MAP message specifies which SID or cable modem has control of upstream communications on a particular frequency channel during each TDMA time slot. The MAP message also specifies the time at which the time slot begins and which interval usage code or burst type is to be used. The number of minislots allocated for a particular time slot is determined, for example, by taking the difference between the current TDMA time slot and the next TDMA time slot.

Ranging in power, slot timing and carrier frequency, as described above, is important in this TDMA communication system. Power control is required in order to normalize receive

power at the cable modem termination system, so as to mitigate inter-channel interference. Controlling carrier frequency ensures proper channelization and the frequency domain for upstream communications. Collisions between data packets and the time domain are mitigated by adjusting slot timing to account for different propagation delays between the cable modem termination system and each individual cable modem on a given frequency channel.

Besides the upstream adjacent channel noise or interference sources which effect power, time and carrier frequency offsets, the upstream channel is also affected by other channel impairments, such as radio frequency interference (RFI) noise. In order to maintain adequate channel quality, channel error characteristics are monitored over time so that as the channel improves or degrades, usage may be adapted, as discussed above. High level channel adaptation algorithms use these parameters to preempt upstream channel failure by increasing forward error correction (FEC) coding gain, changing guard times and/or changing frequency. Since the upstream channel consist of many TDMA point-to-point links, the channel parameters are derived from a statistical analysis of simple accumulated measures such as FEC error and packet error statistics, as described above.

In order to support such channel quality maintenance features, the burst receiver and the MAC, according to the present invention, communicate appropriate information.

According to the present invention, MAC data is broken into FEC blocks, each FEC block is encapsulated with 2 status bytes and 0 to 46 bytes prepend information, status byte fields are used to pass error information and enable statistics calculation and prepend data contains ranging offsets and indicates when ranging is required, as discussed in detail below.

According to the present invention, three individual interfaces between the medium access control (MAC) layer and the physical layer (PHY) or burst receiver are provided. These three individual interfaces are a shared purpose interface, e.g., either an SPI or I2C, a time critical serial interface for specifying TDMA burst information such as the station or service identifier (SID) and the interval usage code (IUC), and a dedicated data interface which is used to pass raw data and in-band control messages, as discussed in detail below.

The shared general purpose interface, typically either a SPI or an I2C, is used to configure non-time critical parameters such as burst profiles, configuration parameters and reading status.

The upstream data is transmitted from the PHY or burst receiver to the MAC using a dedicated 3-wire data interface. This interface includes a serial data line, a free-running serial clock and a burst valid indicator. Since the upstream data is processed in blocks, a single upstream transmission may be transmitted between the burst receiver and the MAC as a series of bursts at the serial clock rate. In addition to the serial data, the MAC needs additional information including identification as to which MAC/PHY bursts belong to which TDMA slot, as well as other information indicating error quality of the received TDMA transmission.

For request and request/data regions, the demodulator of the burst receiver is expecting to receive multiple packets during the interval, and there will be multiple Receive_now signals which are received by the demodulator of the burst receiver.

As shown in FIG. 9, there is a request interval of 6 minislots and it is assumed that each upstream request message will need 2 minislots in order to transmit. Therefore, there will be a

total of three Rx_now signals perceived by the demodulator of the burst receiver. These Rx_now signals are located with offsets of 0, 2 and 4 minislots from the beginning of the interval.

Referring now to FIG. 18, it is important to note that if the first block of a TDMA transmission bit is set, then the prepend information includes 2 status bytes, 4 timestamp bytes 1 channel ID byte, 2 SID bytes, 2 power bytes, 2 frequency bytes and 3 time bytes. The power bytes, frequency bytes, and time bytes include a total of 7 bytes utilized for ranging offsets.

Referring now to FIG. 19, if the equalizer prepend bit is set, then the prepend information is increased by 32 bytes to provide a total length of 48 bytes, include 2 status bytes, 4 timestamp bytes, 1 channel ID byte, 2 SID bytes, 2 power bytes, 2 frequency bytes, 3 time bytes and 32 equalizer coefficient bytes. Again, the power bytes, frequency bytes and time bytes define 7 bytes utilized for ranging offsets.

Referring now to FIG. 20, statistics are kept using counters as shown. These statistics are based upon bits [7:5] of the status bytes.

There are two important concepts with respect to the design of the MAP control interface of the MAC. The first important concept regards the processing of downstream MAP messages, wherein conversion from a format which is specified for the MCNS Data-Over-Cable Service Interface Specification (DOCSIS) to a simplified format which is easy for the MAC to process. The second concept regards the set of control signals which are communicated between the MAP interface and the burst demodulator, including how the signals are toggled so as to convey to the burst demodulator information such as when to receive a packet, the service ID (SID) associated with an incoming packet, the expected length of the region where the packet is going to show up (the time slot for the data packet), and the packet type.

Upstream bandwidth is divided into minislots, which are the smallest time unit utilized by the MAP for bandwidth requests and grants. The exact number of bytes per minislot is typically variable and is usually programmed into the MAC and the burst demodulator via a generic CPU interface or the like. In order to define the minislot reference for the burst demodulator, the MAC provides a signal called the minislot clock (MSCLK) to the burst demodulator. Each rising edge of the minislot clock signal defines the beginning of a new minislot as shown in FIG. 9.

An upstream interval generally consists of an integer number of minislots. There are a plurality of different types, e.g., six different types, of intervals currently defined by the MCNS DOCSIS specification, which include a request interval, an initial maintenance interval, a station maintenance interval, a short data interval, a long data interval, and a request/data interval, as discussed in detail below. The relationship of the request interval, maintenance interval and short and long data intervals with respect to their minislots and the minislot clock is shown in FIGs. 9 and 14-16.

As discussed above, the MAP message contains the upstream for partitioning information which is essential for the burst demodulator to perform the task of receiving upstream packets. A message filter module is designed to snoop all downstream packets and filter out the MAP messages contained therein. The format of the MAP messages is simplified after such filtering.

FIG. 10, shows MAP message format prior to MAP message filtering and FIG. 11 shows MAP message format after MAP message filtering, as discussed in detail below.

By encapsulating each MAC/PHY block with this 2 byte header, the PHY or burst receiver can pass in-band control information to the MAC. The MAC can then use the prepended information to collect channel statistics, as well as pass link related information to higher processes, such as ranging required. This in-band control allows the headend to sense impending channel failure before such failure actually happens, thereby avoiding catastrophic data loss.

Referring now to FIG. 21, the upstream MAC/PHY interface, between the headend (HE) or cable modem termination system (CMTS) MAC 13 and the demodulator 11a of the burst receiver is shown. As discussed above, this interface includes a serial data interface 320, an SPI (or I2C) interface 330 and a serial control interface 240. The serial data interface 240 facilitates the communication of upstream data, including prepended information, from the burst receiver to the MAC. The SPI interface 330 is utilized for general configuration of the MAC and/or burst demodulator. The serial control interface 240 is a time critical interface utilized for the transmission of time critical MAP information from the MAC to the burst demodulator.

According to the present invention, MAC data is broken into forward error correction (FEC) blocks. Each FEC block is encapsulated with 2 status bytes and 0 to 46 bytes of prepend information. Status byte fields are used to pass error information and to enable statistics calculation. The prepend data contains ranging offsets and optional equalizer coefficients.

The upstream data is transmitted from the PHY (burst demodulator) 11a to the MAC 13 using a dedicated 3-wire serial data interface 320. The dedicated serial data interface includes a serial data line, a free-running serial clock and a burst valid indicator. Since the upstream data is processed in blocks, a single upstream transmission may be transmitted between the demodulator of the burst receiver and the MAC as a series of data bursts at the clock rate. In addition to the serial data, the MAC needs additional information including identification as to which MAC/PHY burst belong to which TDMA slot, as well as other information indicating error quality of the received TDMA transmission.

Referring now to FIG. 22, the free-running bit clock 300, the burst valid indicator 301, and the serial data line 302 having prepended information 303 and data 304 thereon, are shown.

Referring now to FIG. 23, the format of the prepended data with equalizer coefficients is shown. The prepended data includes 2 bytes of status flags 250, 4 bytes of timestamp 252, a 1 byte channel ID 254, a 2 byte station or service identifier (SID) 255, 7 bytes of ranging offset and 32 bytes of equalizer coefficients. Using these prepend information, error conditions of the packet may be determined and the PHY parameters may be passed to higher level processes. Channel condition statistics may also be maintained.

Referring now to FIG. 24, the subscriber PHY interface includes two important concepts. First, control information is prepended to the actual packet data 360. This prepended information includes a burst-type byte 362 and a packet length 363, generally of 2 bytes.

The subscriber re-programs the PHY for each individual burst. Since this re-programming may require the exchange of significant amounts of data and must be done in real time, a particular architecture has been developed. A non-real-time general purpose interface is

used to program burst types which are identified by a short ID (burst type). Only the ID and length are transferred in real-time in order to effect immediate re-programming without being impacted by the speed of external interfaces. Real-time control data is piggybacked on the transmit data interface so as to reduce complexity.

Referring now to FIG. 25, an initialization process is generally utilized wherein a plug-and-play-like sign-on sequence is utilized between the headend or cable modem termination system 8 which includes the burst receiver 11 and MAC 13 (FIG. 1) and the subscriber or cable modem 9. According to this initialization process, a timebase messages 401, a default configuration message 402 and a sign-on message 403 are communicated from the cable modem termination system 8 to the cable modem 9 during initialization. A default configuration message is sent for each downloaded frame and the timebase message and default configuration message facilitate upstream time configuration.

A sign-on message 403 transmitted from the cable modem termination system 8 to the cable modem 9 facilitates contention based ranging performed upon a dedicated channel. Typically, the cable modem 9 responds with a sign-on response message 404. Then ranging 405 is initiated by the headend 8 to determine slot timing corrections, carrier frequency corrections, and power corrections. Ranging calibration responses 406 are transmitted from the cable modem 9 to the headend 8.

Service channel, logic address and encryption key information are transferred between the cable modem termination system 8 and the cable modem 9 via re-provision message 407 transmitted from the cable modem termination system 8 to the cable modem 9 and via re-provision response message 408 transmitted from the cable modem 9 to the cable modem termination system 8. When the process is complete, an initialization complete message 409 is transmitted from the cable modem termination system 8 to the cable modem 9.

Referring now to FIG. 26, the MAC framing and the PHY or burst receiver framing are decoupled and upstream frame synchronization is based on timestamp messages. The cable modem 9 generates a timestamp message which is utilized by a subscriber cable modem 8 to effect timing synchronization such that proper slot timing is facilitated. The output from a headend timing generation circuit is reduced in frequency by a divider 450 and is used by a timestamp counter 451 to generate slot/frame timing 452. The slot/frame timing is transmitted via continuous modulator 470 through analog front end 471 over a desired downstream frequency channel 472, typically utilizing a hybrid fiber coax (HFC) network to the analog front end 473 of a desired subscriber cable modem 8. A continuous demodulator 474 demodulates the slot/frame time and provides it to a timing recovery circuit 475 which utilizes a timestamp detector 476 to provide the slot/frame timing to a digital timing loop defined by loop filter 477, numerically controlled oscillator 478 and local timestamp counter 479. The loop generates slot/frame timing for use by the subscriber cable modem 8 and generating upstream TDMA messages.

Thus, the subscriber cable modem 8 is capable of transmitting upstream data via burst modulator 458 and analog front end 457 in a desired upstream channel 456, typically via a hybrid

fiber coax (HFC) network to the analog front end 455 of the cable modem termination system, wherein the message is demodulated by burst demodulator 11a.

Referring now to FIG. 27, the MAP serial interface (MAC to PHY) field definition includes a service ID 501 of 14 bytes, a slot type 502 of 4 bytes and a slot region length 503 of 14 bytes.

Referring now to FIG. 28, the prepended information (form PHY to MAC) includes status information 510 of 2 bytes, minislot control 511 signal of 4 bytes, a channel ID 512 of 1 byte, a station or service identifier (SID) 513 of 2 bytes, ranging information 514 of 7 bytes and equalizer coefficients 515 of 32 bytes.

Referring now to FIG. 29, each MAC/PHY burst is tagged with 2 status bytes as indicated.

Referring now to FIG. 30, burst demodulator status processing flow is shown. Forward error correction (FEC) 520 and demodulation information 524 are added to prepended information 571, and receiver TDMA control 523 is provided by MAP interface 522. The forward error correction 520 information includes forward error correction statistics such as: no forward error correction errors (No_FEC), correctable forward error corrected errors (Corr_FEC Err), and uncorrectable forward error correction errors (Uncorr_FEC_Err).

The MAP interface information 522 includes service slot type information. The receiver TDMA control 523 includes information indicative of the first and last block of information. The demodulator information 524 includes unique word detected, ranging information and equalizer coefficients.

Referring now to FIG. 31, the burst demodulator SPI bus interface is shown. The SPI interface 330 provide set-up information to configuration registers 560. The set-up configuration includes the carrier frequency, the baud rate, the minislot size, the required packet size, and ranging thresholds.

The SPI interface 330 also provides burst configuration information to burst configuration registers 562 via multiplexer 563 and data registers 564, 565 and 566. The burst configuration information includes unique word pattern, unique word window, QAM mode, forward error correction parameters, such as N, K and T, guard time, de-randomizer information, differential encoding information, preamble length and equalizer training length.

Referring now to FIG. 32 (a detailed drawing of FIG. 24), the generic byte base serial input interface at the upstream MAC/PHY interface at the subscriber cable modem with control information prepended and TXS2P=1, includes the standard ATM signals of transmit clock (TX CLK) 601a, transmit enable bar (TX_ENABLE bar) 602a, transmit cell available (TX_CLAV) 603a, transmit start-of-cell (TX_SOC) 604a, and transmit data (TX_DATA) 605a. When the control bit, TXS2P is set to equal 1, then transmitted data (TX_DATA) 605a is transmitted most significant bit (MSB) first.

Referring now to FIG. 33 (another detailed drawing of FIG. 24), the transmit clock (TX CLK) 601b, transmit enable bar (TX_ENABLE bar) 602b, transmit cell available (TX_CLAV) 603b, transmit_start-of-cell (TX_SOC) 604b and transmit data (TX_DATA) 605a are show when

TXS2P is set to zero. When TxS2P is set to 0, then the least significant bit (LSB) is transmitted first.

Although the present invention is described and illustrated herein as providing acquisition in 16 symbols or less, the present invention may also be utilized to provide acquisition in greater than 16 symbols. For example, the present invention may be utilized to provide acquisition and 24 symbols. Thus, use of the present to provide acquisition and 16 symbols or less is by way of example only and not by way of limitation.

It is understood that the exemplary MAC/PHY interface described herein and shown in the drawings represents only a present embodiment of the invention. Indeed, various modifications and additions may be made to such embodiment without departing from the spirit and scope of the invention. Thus, these and other modifications and additions may be obvious to those skilled in the art and may be implemented to adapt the present invention for use in a variety of different applications.

Method and Apparatus for Reducing Noise in a Bidirectional Cable Transmission System

In FIG. 1 a bidirectional radio frequency (RF) cable transmission system has a large number of user terminals connected by a cable network to a headend or a cable modem termination system (CMTS). Cable modems (CM_1, CM_2,...CM_n) are located at the respective user terminals. An RF transmitter 10 and an RF receiver 12 are located at the headend. RF transmitter 10 is connected by a number of downstream channels 14 of the cable network to cable modems CM_1, CM_2,...CM_n. Cable modems CM_1, CM_2,...CM_n are connected by upstream channels 16 to RF receiver 12. As represented by blocks $H_1(f)$, $H_2(f)$,...$H_n(f)$, the individual upstream channels 16 are impaired by user specific noise associated with the respective cable modems such as multi-path reflections and the like. In addition, as represented by a summing junction 18, upstream channels 16 are also impaired by common noise such as, ingress noise, during upstream transmission. The invention reduces the common noise symbolized by summing junction 18 and the individual noise symbolized by $H_1(f)$, $H_2(f)$,...$H_n(f)$.

As shown in FIG. 2, RF receiver 12 at the headend has a down converter 20 that shifts the RF signal on the selected upstream channel 16 to baseband. After passing through a matched filter 22, the baseband signal is coupled to an adaptive notch filter 24, which is described in more detail below in connection with FIG. 3. Adaptive notch filter 24 is coupled by a demodulator 26 to a generalized decision feedback equalizer (DFE) 28, which is described in more detail below in connection with FIG. 4. The output of DFE 28 is connected to a slicer 30, which determines the quantized value of the signal. The output of slicer 30 is fed to forward error correction (FEC) circuitry 32. The output of FEC 32 is the transmitted data in binary form.

As illustrated in FIG. 3, adaptive notch filter 24 is a linear monic filter having a fixed main tap 34 represented by the coefficient b0 and a plurality of successive variable taps 36 represented by coefficients b1, b2, ..., bn. Taps 34 and 36 feed a summing junction 38.

As illustrated in FIG. 4, generalized DFE 28 comprises a feed-forward equalizer 40 and a feedback equalizer 42 that feed a summing junction 44. The output of summing junction 44 is coupled to a slicer 46, which determines the quantized value of the signal applied to decision

feedback equalizer 28. The output of slicer 46 is coupled to the input of feedback equalizer 42 and to FEC 32 (FIG. 2). As described in more detail below, generalized DFE 28 operates in a special way. That is, rather than obtaining the coefficents of the feedforward and feedback parts together, the coefficients of the feed-forward and feedback parts are trained in a sequential manner. Also, the feedforward equalizer can take a linear equalizer structure where the main tap location can be any tap location.

As illustrated in FIG. 5, each cable modem has a receiver 50 that processes RF signals transmitted on a selected one of downstream channels 14 and a transmitter 52 that sends RF signals to the headend on a selected one of upstream channels 16. A transmit equalizer 54 is connected in series between a modulator 53 inside transmitter 52 and upstream channels 16. As described in more detail below, the coefficients for equalizer 54 are transmitted to receiver 50 at the cable modem on one of downstream channels 14 and coupled by receiver 50 to transmit equalizer 54. Transmit equalizer 54 is also a linear equalizer structure corresponding to the feedforward equalizer at the receiver 40.

FIG. 6 illustrates the TDMA time slots in a selected one of upstream channels. As shown, there are ranging slots 56, requests slots 58, and user data slots 60. There are also idle slots 62, which are unique to the invention. The timing and frequency of slots 56-62 are determined at the headend, which sends out control messages on one of downstream channels 14 assigned to system management to establish a framing structure for the upstream channels. These control messages include information about the type of slot, i.e., ranging, request, data, or idle and the service identifier (SID) which uniquely identifies each cable modem. For a more detailed description of the upstream channel management function, reference is made to U.S. Provisional Application No. 60/106,427 filed on October 30, 1998.

FIG. 7 illustrates a method for operating the apparatus in FIGS. 2-5 so as to cancel common noise such as ingress and to compensate for individual noise such as multipath noise, that impairs upstream channels 16. As depicted by a block 64, an idle slot is created by the headend when the system is powered up and thereafter from time to time whenever it is desired to re-adjust notch filter 24 (FIG 2). The idle slot is part of the upstream TDMA framing structure created at the headend and transmitted to each cable modem on one of downstream channels 14 assigned to system management. The idle slot identifies no cable modem SID and contains no upstream signal. It can be created simply by assigning the SID of a unicast (or reservation) slot to a null value. Since the idle slot is created as part of the TDMA framing structure, its time of arrival at the headend is known. In essence, the idle slot is a known time period during which there is no signal on upstream channels 16. Any energy received at receiver 10 at the headend during this time period represents common noise such as ingress noise. In FIG. 8A, this common noise is illustrated as a noise spike 80 superimposed on the frequency response 81 of the selected channel. As depicted by a block 66, during the idle slot of each of upstream channels 16, the coefficients of adaptive notch filter 24,
$B_1, B_2, \ldots B_{n-1}$, are adjusted to minimize its output by for example an LMS process. The value of main tap B_0 is fixed. This tends to cancel the common noise as illustrated by a notch 82 in FIG. 8B, but introduces signal distortion into the frequency response. As depicted by a block 68, the

coefficients of notch filter 66, namely, B_1, B_2,...B_{n-1}, are impressed upon FBE 42 without change to compensate for the distortion introduced by notch filter 24. FIG. 8C illustrates the resulting frequency response at the output of DFE 28 with a narrow sharp notch that rejects the common noise. FIG. 9A represents a typical spread of signal values in a 16-QAM constellation before common noise cancellation by notch filter 24 and FBE 42. FIG. 9B represents the after case. As depicted by a block 70, the coefficients of notch filter 24 and FBE 42 are frozen until next time that an idle slot is created by the headend so the described apparatus can take into account changes in the common noise in upstream channel 16. During the initial setup at a particular RF frequency chosen by the down converter 20 and when the settings of adaptive notch filter 24 are updated, the corresponding coefficients of notch filter 24, namely, B_1, B_2,...B_{n-1}, for the selected channel are recovered and impressed upon notch filter 24 and FBE 42. As a result, adaptive notch filter 24 and FBE 42 cancel common noise in the selected channel during the data transmission interval that follows. As depicted by a block 72, FFE 40 is adjusted during the ranging process in preparation for upstream data transmission from each cable modem. The common noise has been canceled prior to this adjustment. When the headend assigns a ranging slot to a particular cable modem, the modem sends a packet of ranging data, including a training sequence to the headend. The training sequence is used to derive coefficients for FFE 40. These coefficients represent the frequency shaping required to compensate for the individual noise of the particular cable modem transmitting the ranging packet, i.e., the frequency shaping required to provide a flat frequency response at the output of DFE 28. The calculated coefficients are transmitted with the SID of the cable modem on the one of downstream channels 14 assigned to system management. As depicted by a block 73, these coefficients are applied to transmit equalizer 54 at the selected cable modem. Before the data is transmitted by the cable modem over the assigned one of upstream channels 16, FFE 40 is reset so the taps, except for the main tap, are set to zero. As a result, the apparatus compensates for individual noise by pre-equalization at the transmitting cable modem, while FFE 40 introduces no compensation except simple tracking.

Reference is made to FIG. 10A for a diagram of common noise (such as ingress) spikes 74 and 76 superimposed on the frequency response of one of upstream channels 16. The effect of multi-path is shown by a sag 77 near the middle of the frequency response. FIG. 10B represents the pre-equalizing effect introduced by linear equalizer 54 at the transmitting cable modem. This pre-equalization compensates for sag 77a in FIG. 10A and thus flattens the overall frequency response of the signal arriving at receiver 12. It also adds a notch at the frequencies where ingress noise is present 74a and 76a.

Referring to FIG. 10B, the adaptive notch filter coefficients can be used via FFT processing for dynamic channel allocation with ingress cancellation to measure the inverse of the channel spectrum or to find the location of the ingress noise. This facilitates in estimating the channel quality for selecting an appropriate channel and bandwidth, as shown in FIG. 8 of Robust Technique for Optimal Upstream Communication Between Cable Modem and Headend.

As used in the claims herein, the term "idle slot" is a time period known to the headend in which no signal is being transmitted in the upstream channel. Consequently, any energy detected

in the channel at the headend during this time period is common noise introduced into the cable network.

The described embodiments of the invention is only considered to be preferred and illustrative of the inventive concept; the scope of the invention is not to be restricted to such embodiment. Various and numerous other arrangements may be devised by one skilled in the art without departing from the spirit and scope of this invention.

CLAIMS

1. A method for communicating information, the method comprising:

allocating a time slot in a time division multiple access system for a transmission from a subscriber to a headend the time slot being sufficient for only a first portion of a transmission, a second portion of the transmission being transmitted in other than the first time slot;

enhancing synchronization a clock of the subscriber with respect to a clock of the headend using a message transmitted from the headend to the subscriber which is indicative of an error in a subscriber transmission time with respect to the time slot;

using a feedback loop process to determine at least one of fractional symbol timing correction and carrier phase correction of a transmission from the subscriber to the headend;

monitoring quality of at least one channel and changing modulation in response changes to monitored channel quality;

using information representative of parameters of received time division multiple access data to facilitate processing of the received time division multiple access data in a receiver, the parameters being communicated within the headend; and

generating filter coefficients at the headend from a ranging signal transmitted from the subscriber to the headend and transmitting the filter coefficients from the headend to the subscriber, the filter coefficients being used of the subscriber to compensate for noise in a transmission from the subscriber to the headend.

2. A method for communicating with a cable transmission system comprising:

means for requesting an amount of bandwidth on the cable system to transmit data;

means for receiving a grant of an amount of bandwidth to transmit data in response to the request;

means for comparing the requested amount of bandwidth with the granted amount of bandwidth;

means responsive to the comparing means for fragmenting the data to be transmitted into a plurality of segments if the requested amount is larger than the granted amount, one of the segments being no larger than the granted amount; and

means responsive to the grant for transmitting the data to be transmitted to the cable system if the requested amount is no larger than the granted amount; and

means responsive to the grant for transmitting the one segment to the cable system if the requested amount is larger than the granted amount.

3. A method for synchronizing upstream communications between a plurality of cable modems and a cable modem termination system, the method comprising:

generating a timebase message representative of a frequency of a clock of the cable modem termination system;

generating a slot timing offset message representative of a slot timing offset of the clock of a selected one of the cable modems with respect to the clock of the cable modem termination system;

transmitting the timebase message to the selected cable modem;

transmitting the slot timing offset message to the selected cable modem;

enhancing synchronization of a frequency of the clock of the selected cable modem with respect to the clock of the cable modem termination system using the timebase message;

compensating for the slot timing offset of the clock of the cable modem with respect to the clock of the cable modem termination system using the slot timing offset message; and

repeating the generating, transmitting, enhancing and compensating acts for other ones of the cable modems.

4. A method for acquiring a data packet in a cable modem termination system, the method comprising:

determining fractional symbol timing correction by a feedback loop process;

determining carrier phase correction by a feedback loop process; and

determining fine amplitude correction by an estimation process.

5. A method for communicating modulated information from a plurality of cable modems to a cable modem termination system, the method comprising:

monitoring a plurality of upstream channels for at least one parameter which is indicative of channel quality; and

adjusting the modulation in response to the channel quality parameter.

6. A method for processing received time division multiple access data, the method comprising:

communicating information from a MAC to a burst receiver, the information being representative of parameters of the received time division multiple access data; and

using the information communicated from the MAC to the burst receiver to facilitate processing of the received time division multiple access signal.

7. In a cable system having a headend and a plurality of user terminals interconnected by a cable that has a single downstream transmission path from the headend to each of the user terminals and a plurality of upstream transmission paths from each of the users terminals to the headend, a method for canceling common noise and compensating for individual noise in the upstream transmission paths, the method comprising the steps of:

adjusting a notch filter at the headend to reject one or more bands of common noise;

compensating for distortion caused by the notch filter at the headend;

after the adjusting and compensating steps, receiving a ranging signal at the headend from each user terminal;

generating transmit equalizer coefficients for each user terminal from the ranging signals;

transmitting the pre-equalizer coefficients to the respective user terminals; and

applying the filter coefficients to a transmit equalizer at the respective user terminals to compensate for individual noise at the respective user terminals.

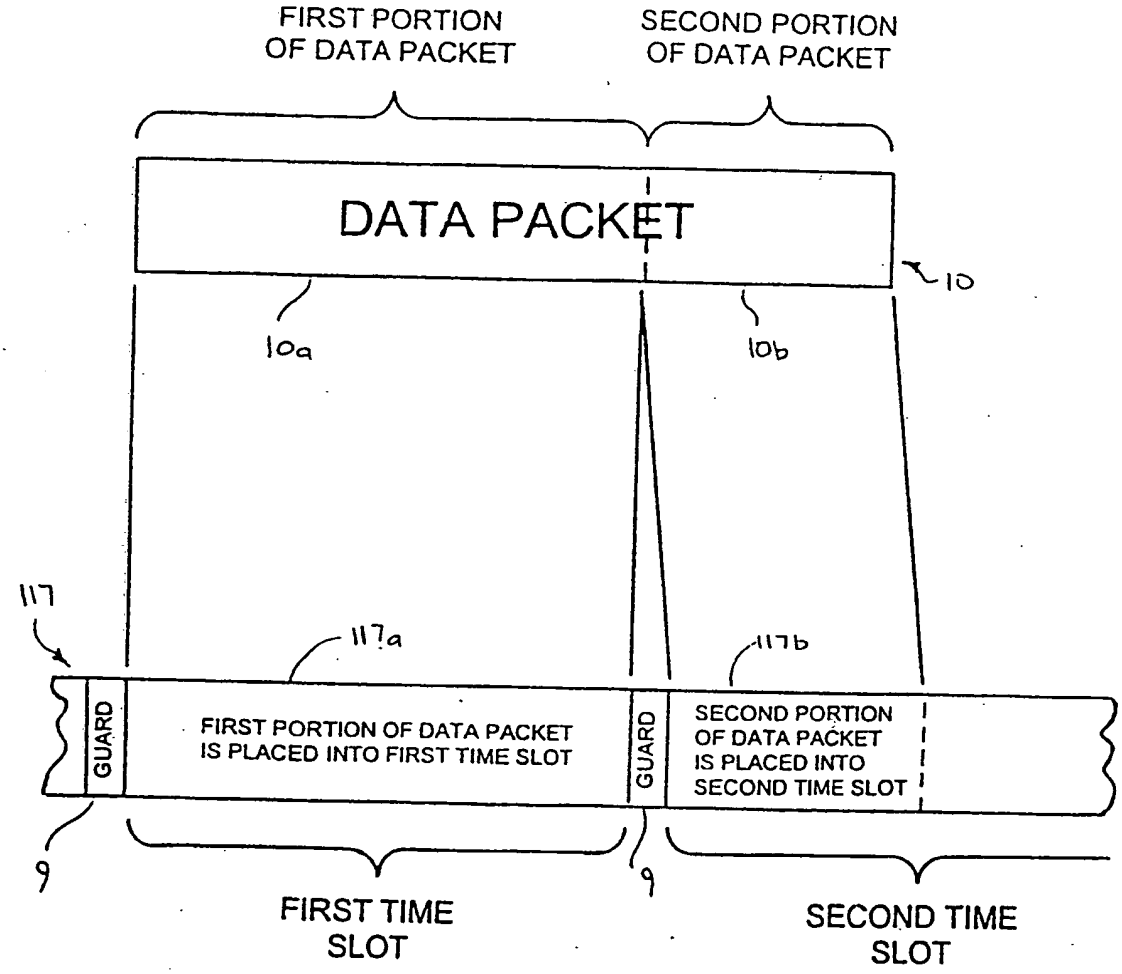


FIG. 1

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

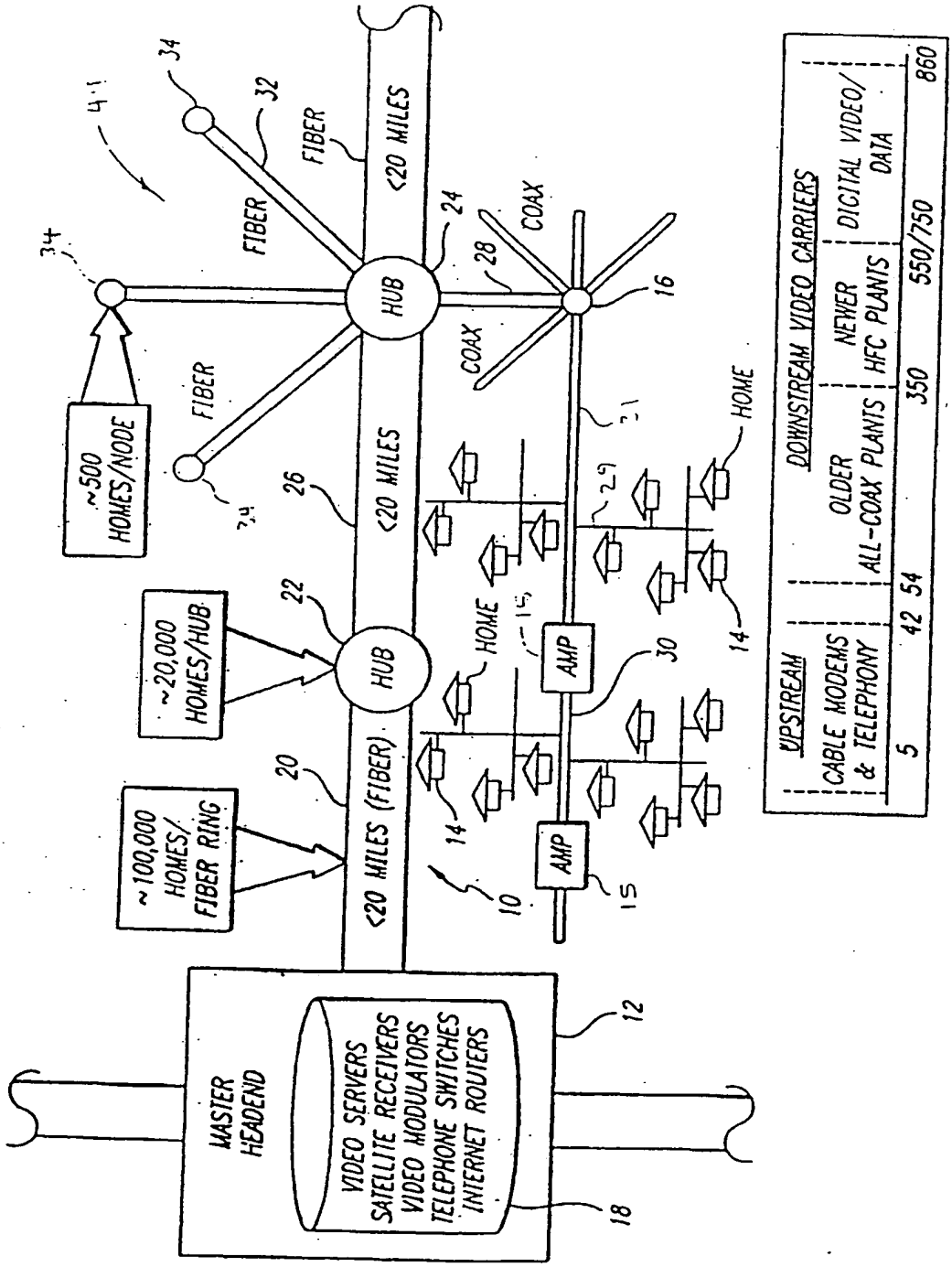


FIG. 2

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

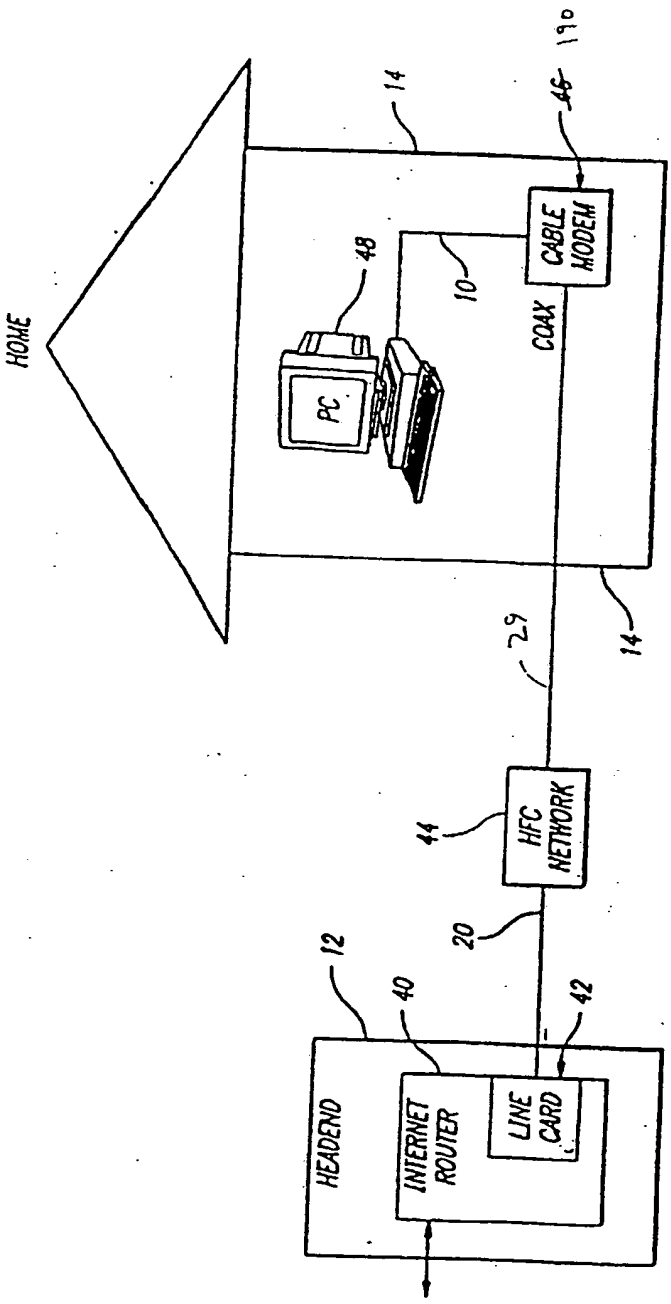


FIG. 3

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

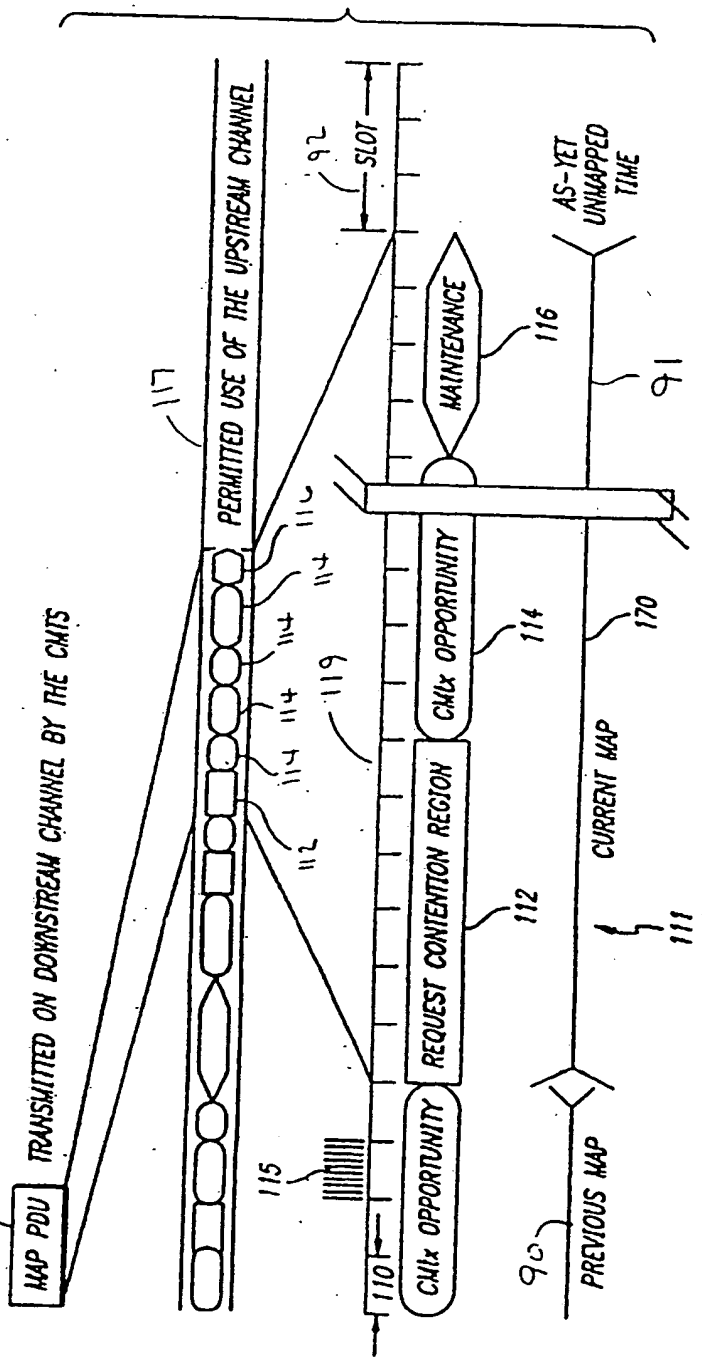


FIG. 4

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

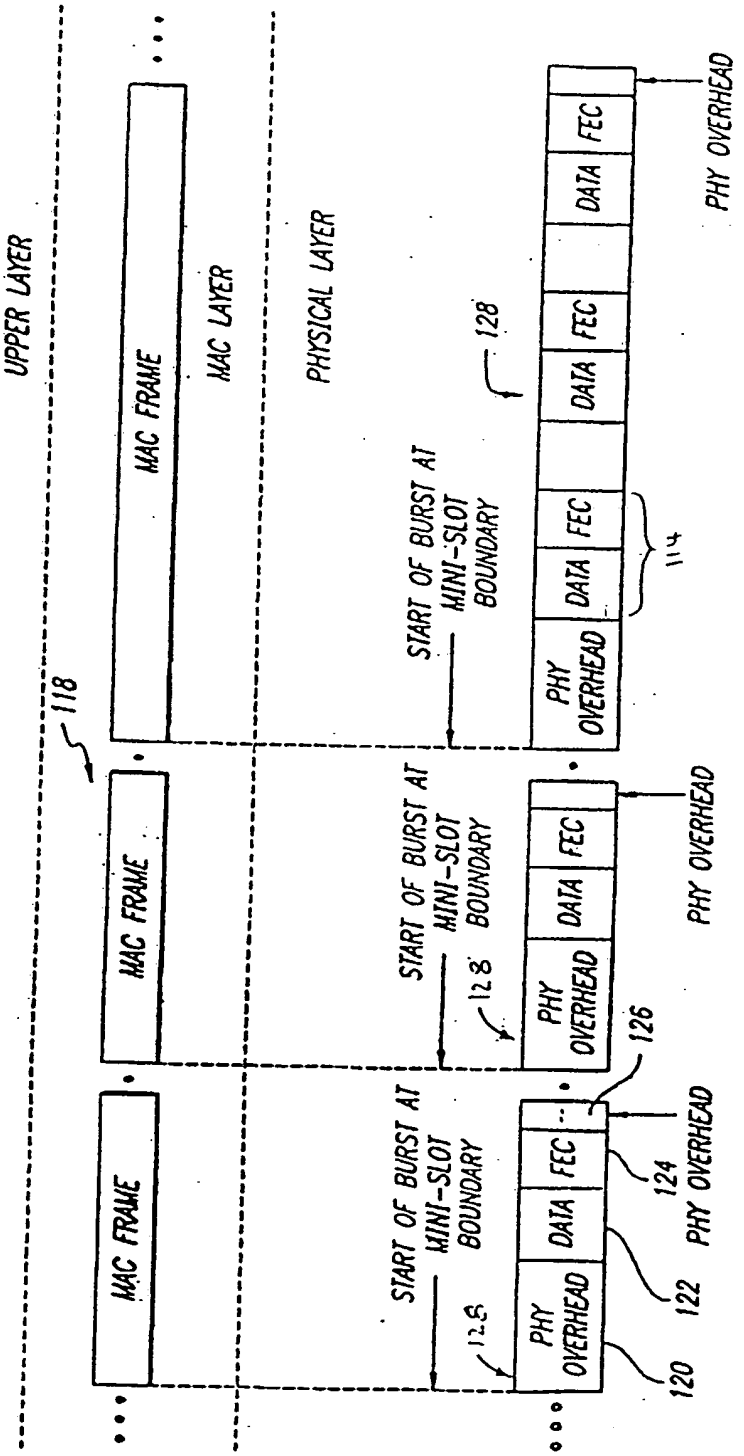


FIG. 5

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

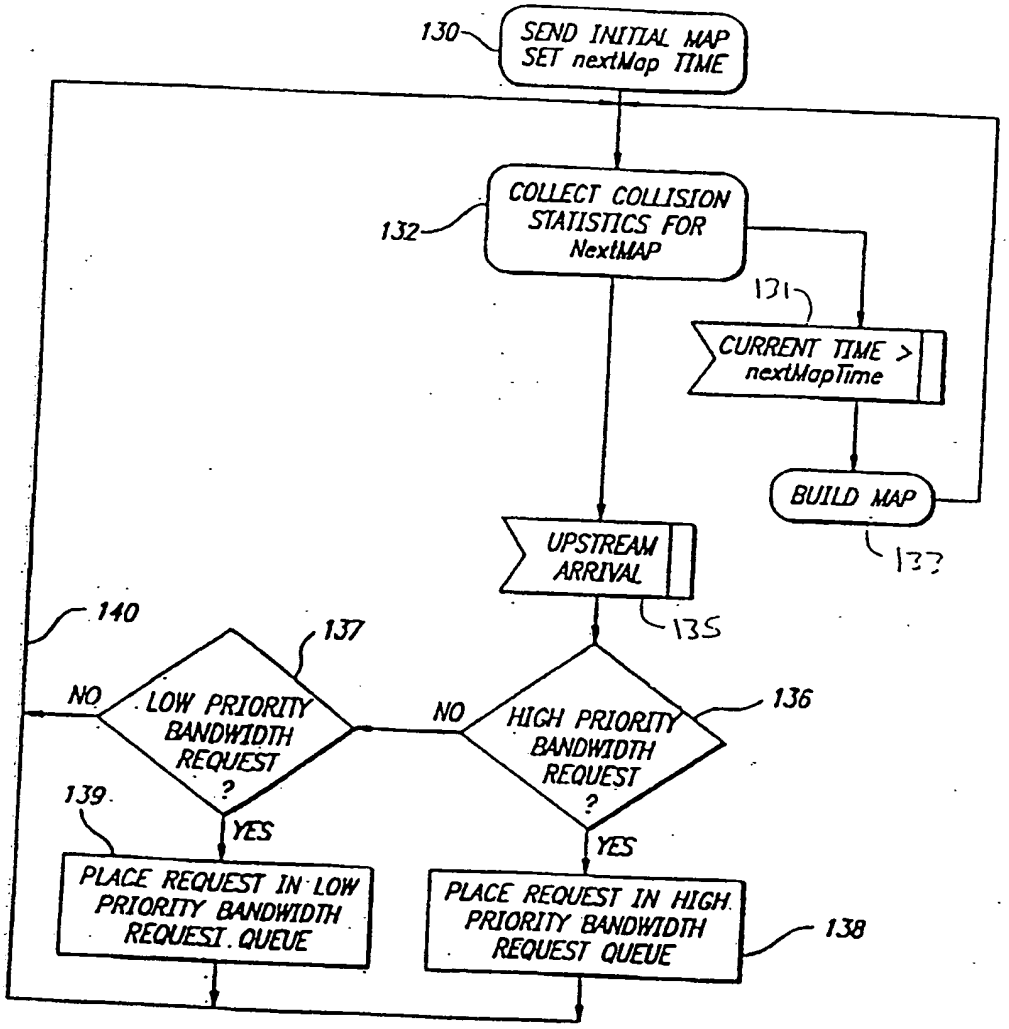


FIG. 6

DATA PACKET
FRAGMENTATION IN A
CABLE MODEM SYSTEM

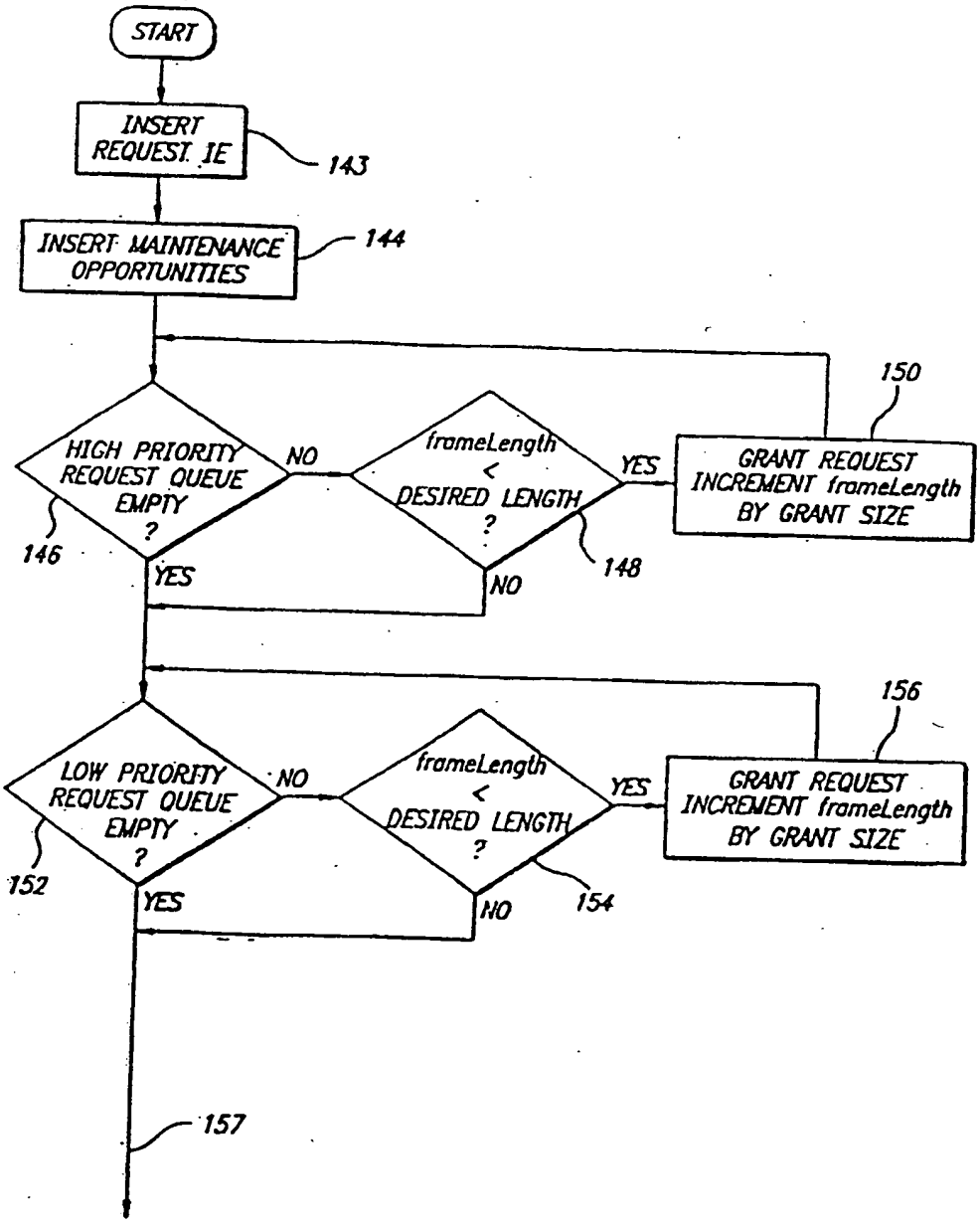


FIG. 7

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

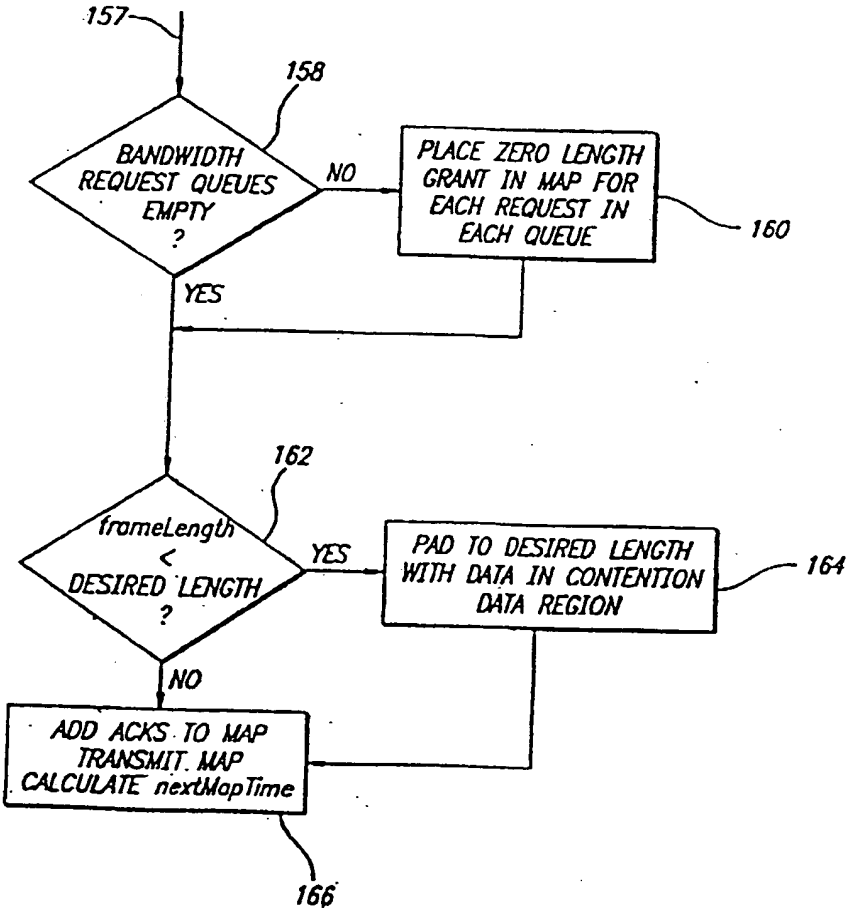


FIG. 8

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

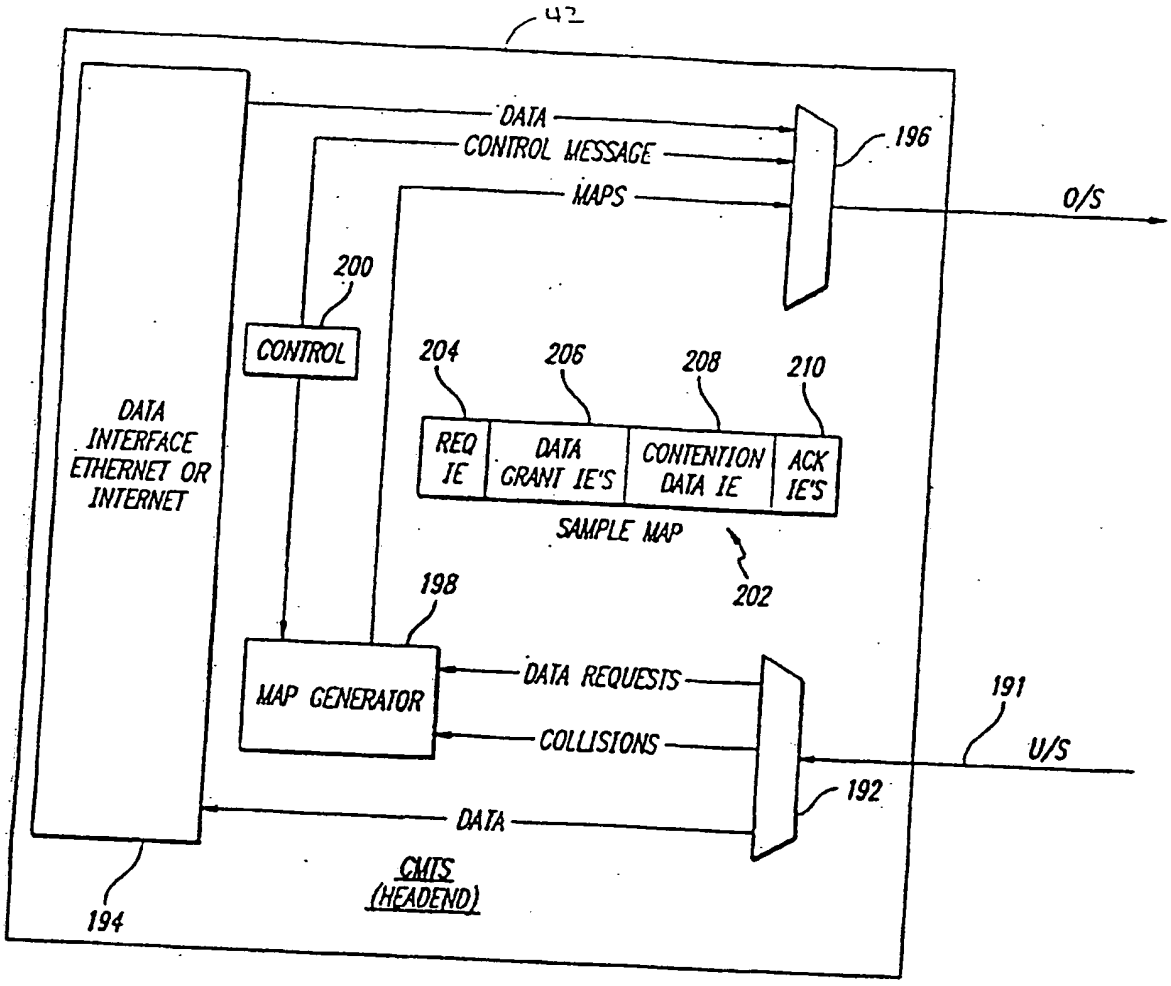


FIG. 9

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

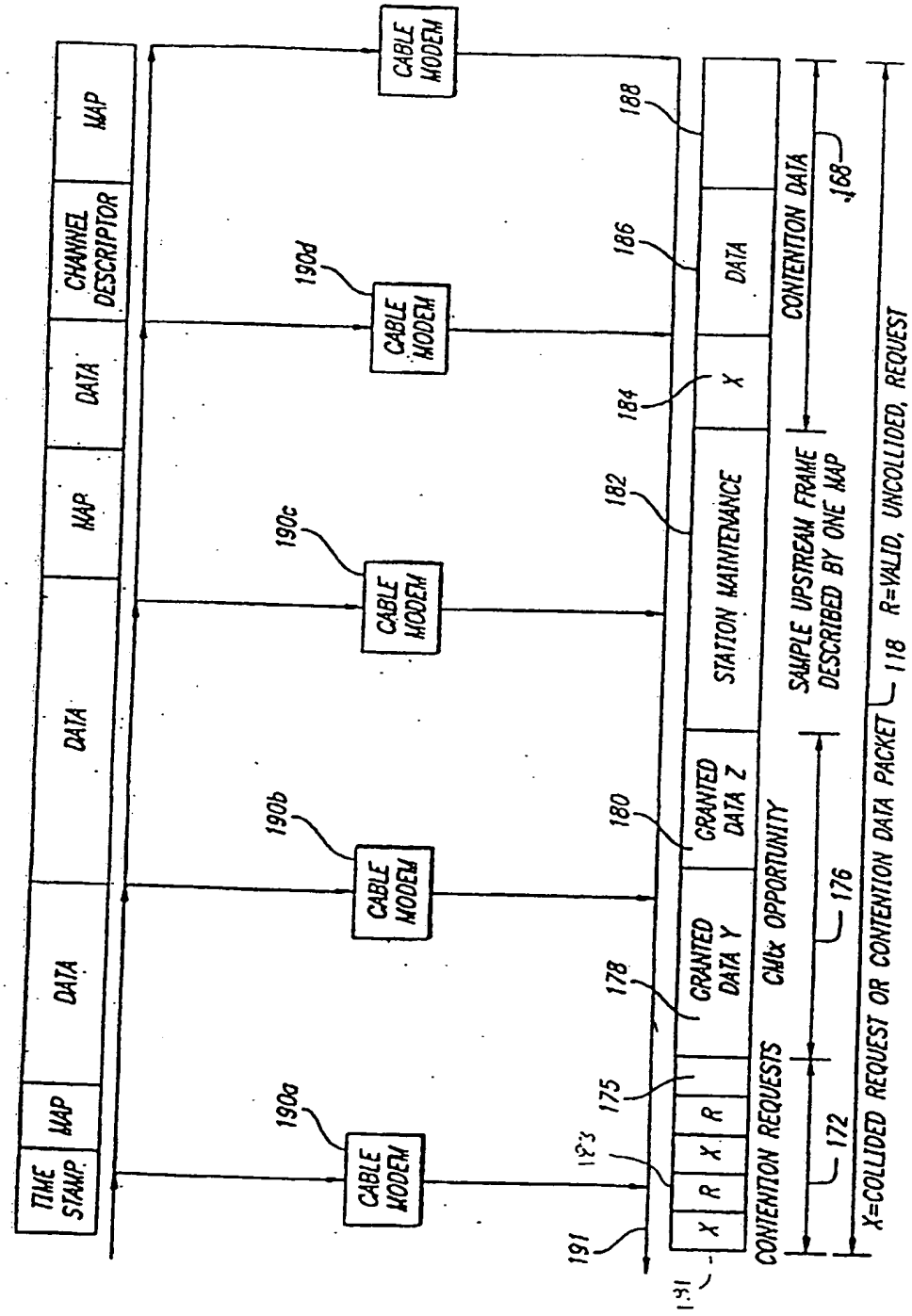


FIG. 10

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

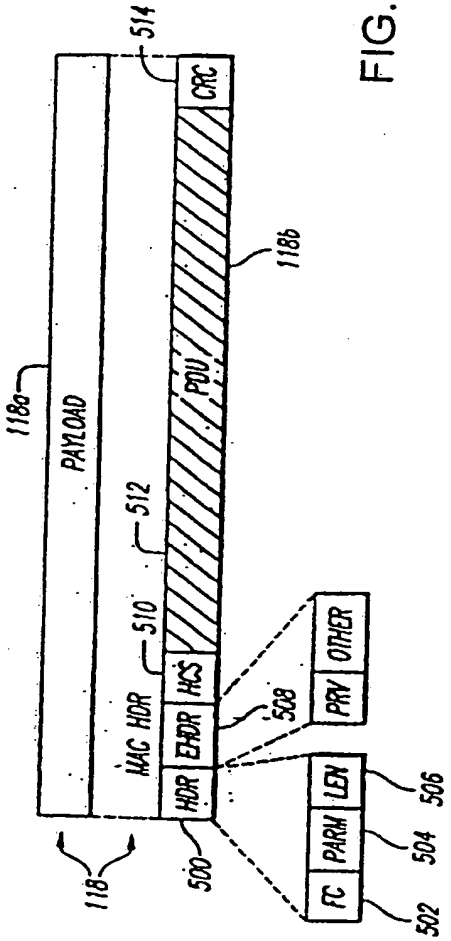


FIG. 11

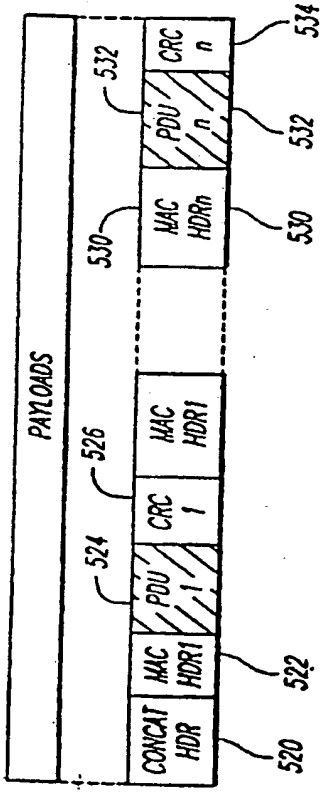


FIG. 12

DATA PACKET
FRAGMENTATION IN A
CABLE MODEM SYSTEM

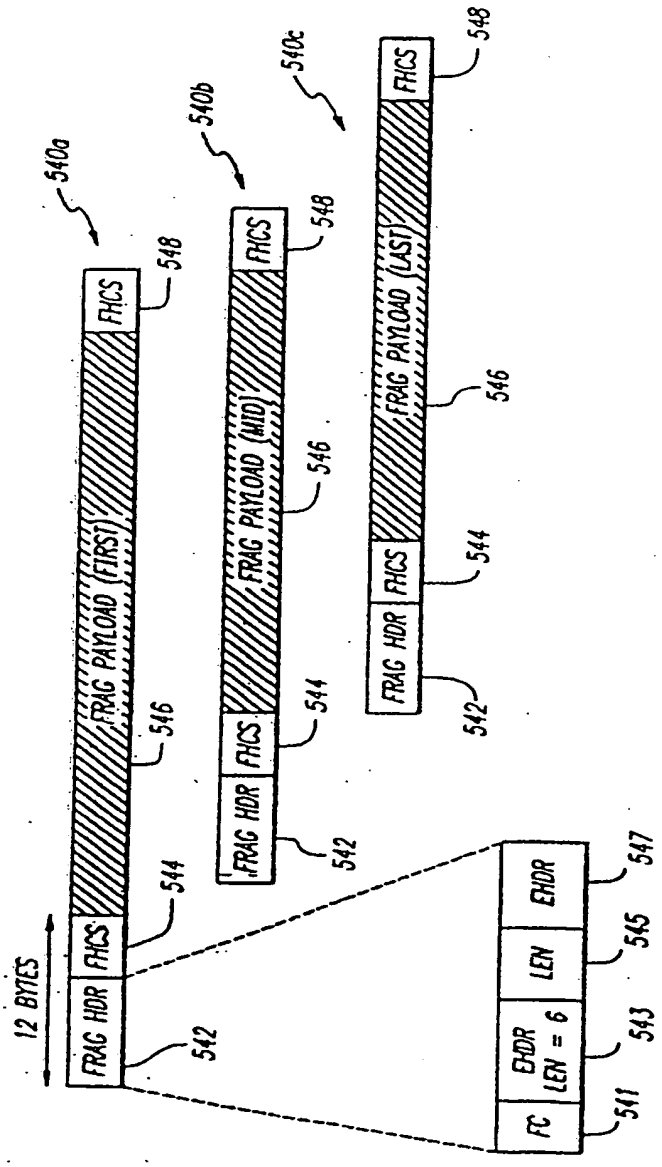


FIG. 13

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

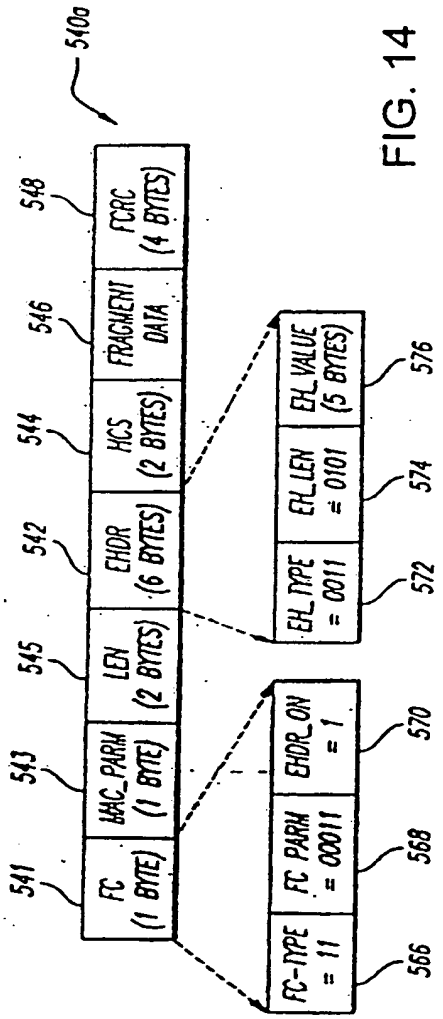


FIG. 14

FIELD	USAGE	SIZE
FC	FC_TYPE = 11;MAC-SPECIFIC HEADER FC_PARM [4:0] = 00011;FRAGMENTATION MAC HEADER EHDR_ON = 1;FRAGMENTATION EHDR FOLLOWS	8 BITS
MAC_PARM	ELEN = 6 BYTES;LENGTH OF FRAGMENTATION EHDR	8 BITS
LEN	LEN = n + 10;TOTAL LENGTH OF THIS FRAGMENT INCLUDING PAYLOAD, EHDR, FCRC	16 BITS

FIG. 15

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

FIELD	USAGE	SIZE	
EHDR	EH_TYPE=3;SAME TYPE AS BP_UP	4 BITS	6 BYTES
	EH_LEN=5;LENGTH OF THIS EHDR	4 BITS	
	KEY_SEQ;SAME AS IN BP_UP	4 BITS	
	VER=0001;VERSION NUMBER FOR THIS EHDR	4 BITS	
	ENABLE IF ENABLE=0, BPI DISABLED IF ENABLE=1, BPI ENABLED	1 BIT	
	TOGGLE BIT;SAME AS IN BP_UP	1 BIT	
	SID;SERVICE ID ASSOCIATED WITH THIS FRAGMENT	14 BITS	
	REQ;NUMBER OF MINI-SLOTS FOR A PIGGYBACK REQUEST	8 BITS	
	RESERVED;MUST BE SET TO ZERO	2 BITS	
	FIRST_FRAG;SET TO ONE FOR FIRST FRAGMENT ONLY	1 BIT	
	LAST_FRAG;SET TO ONE FOR LAST FRAGMENT ONLY	1 BIT	
	FRAG_SEQ;FRAGMENT SEQUENCE COUNT, INCREMENTED FOR EACH FRAGMENT, SET TO ZERO FOR FIRST FRAGMENT	4 BITS	
HCS	MAC HEADER CHECK SEQUENCE		2 BYTES
FRAGMENT DATA	FRAGMENT PAYLOAD;PORTION OF TOTAL MAC POU BEING SENT		n BYTES
FCRC	CRC ACROSS FRAGMENT PAYLOAD		4 BYTES
	LENGTH OF A MAC FRAGMENT FRAME	n + 16 BYTES	

FIG. 16

DATA PACKET
FRAGMENTATION IN A
CABLE MODEM SYSTEM

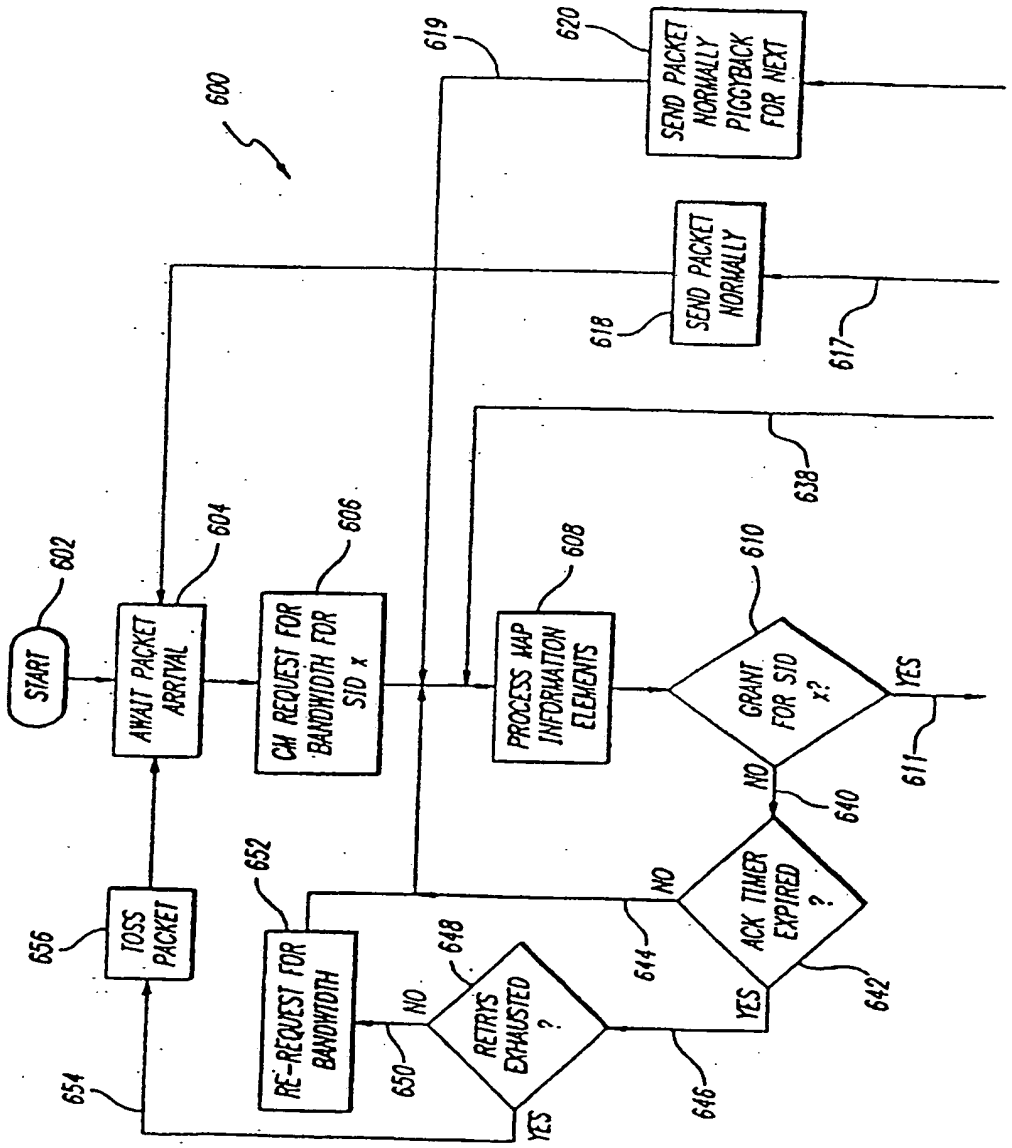


FIG. 17

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

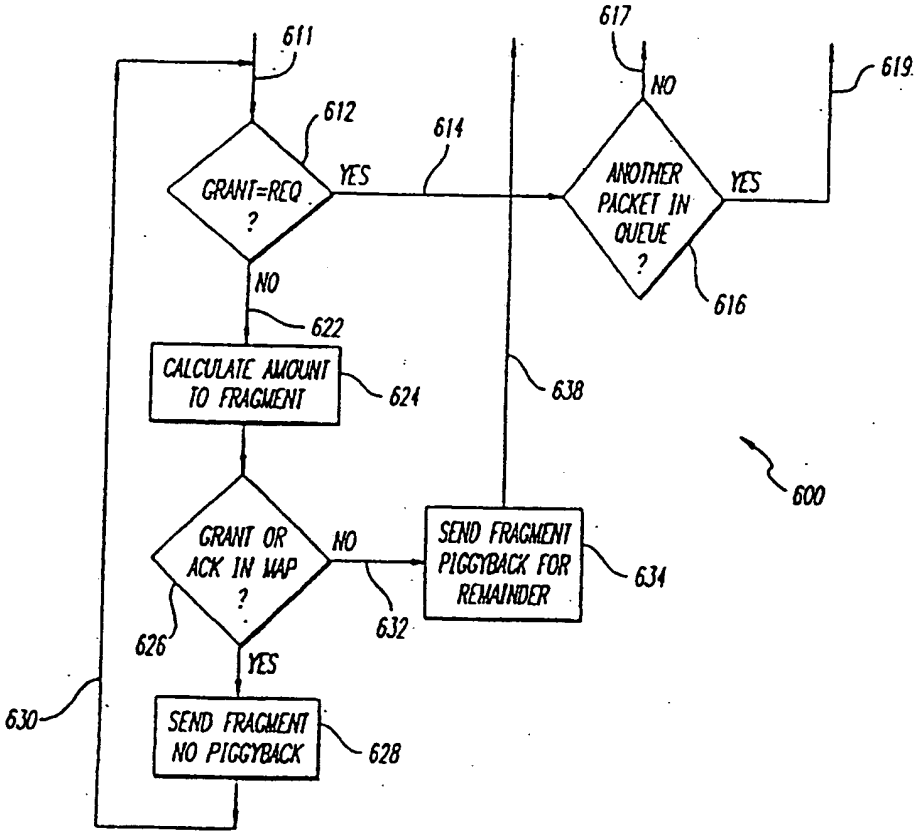


FIG. 18

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

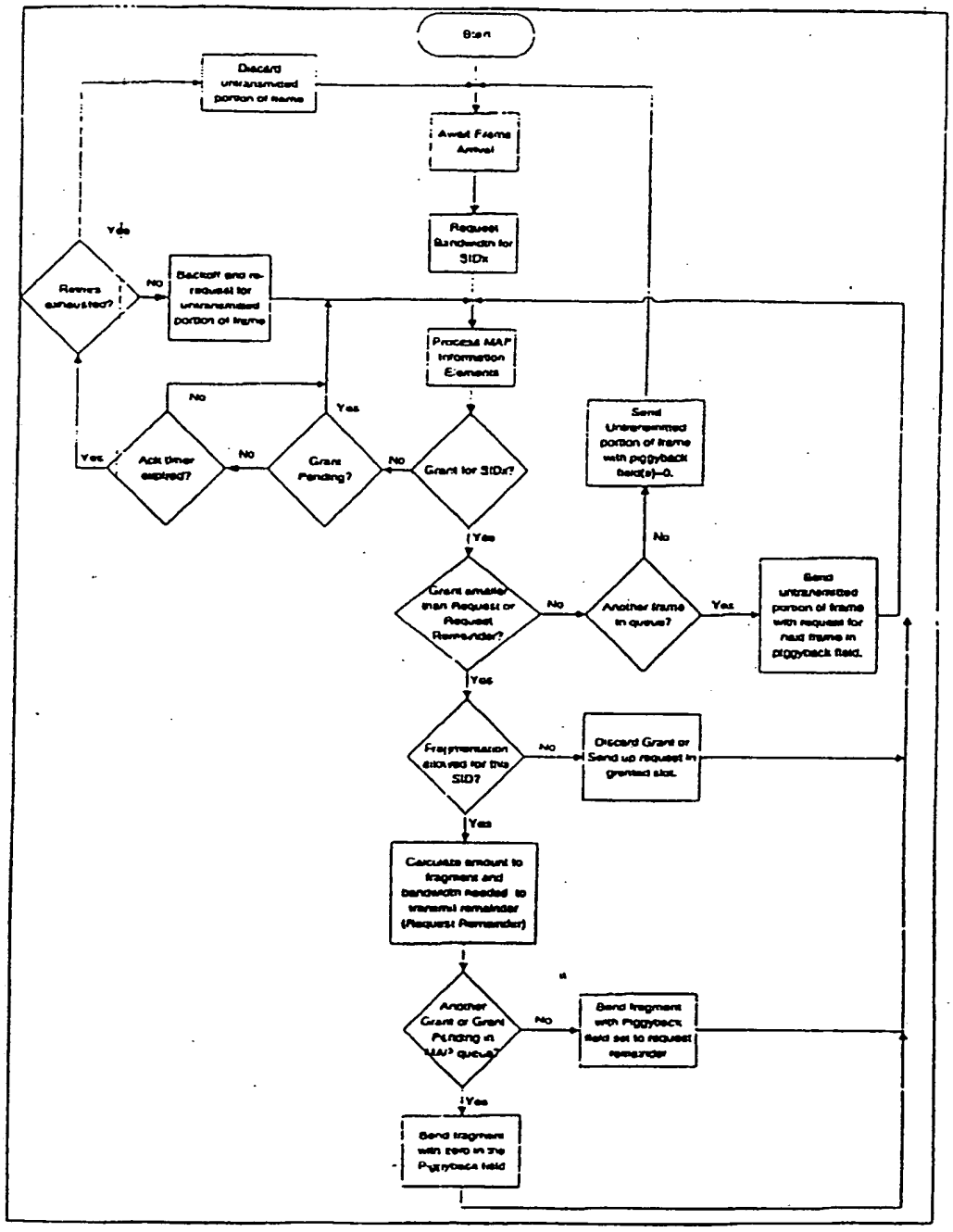


FIG. 19

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

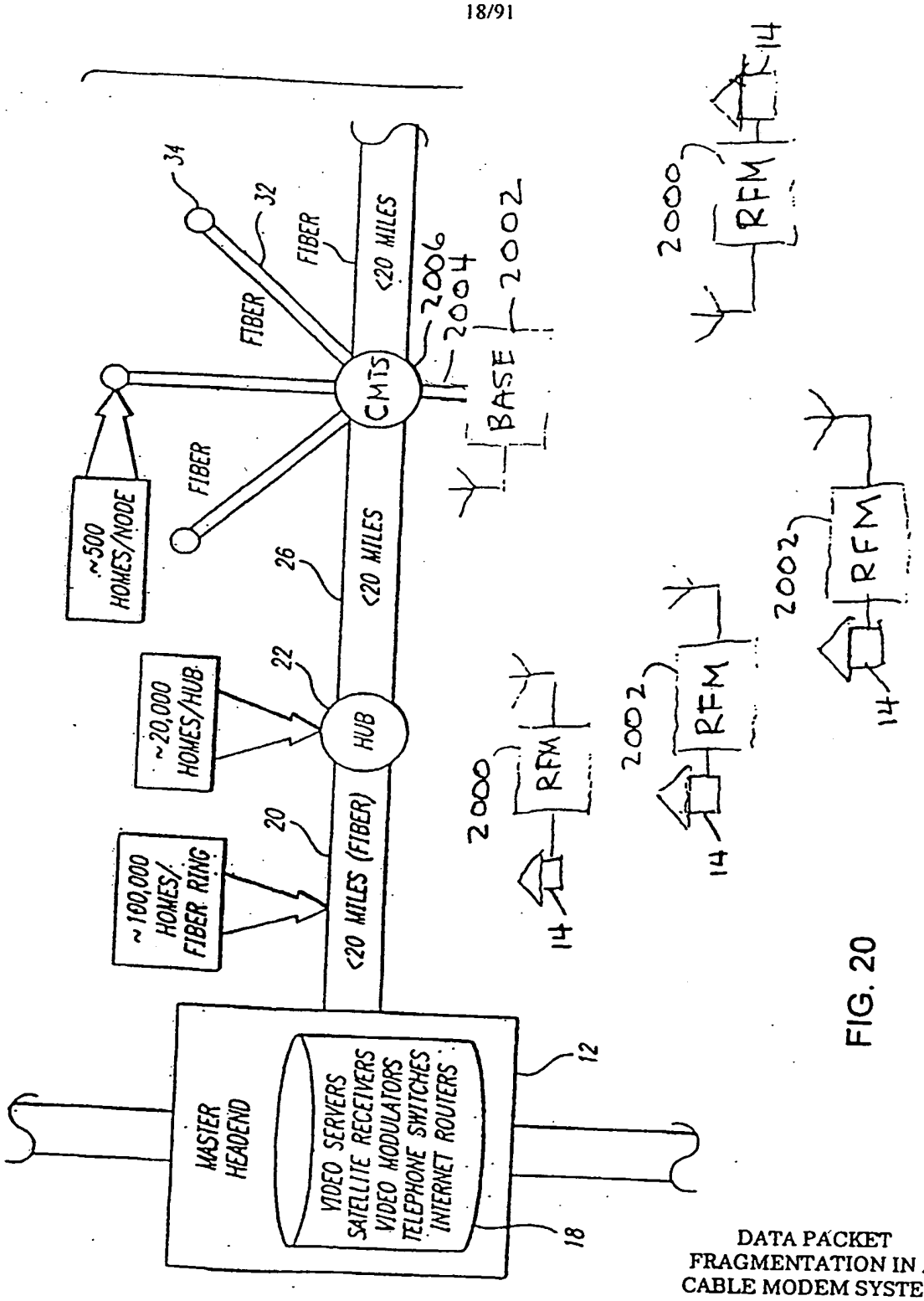


FIG. 20

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

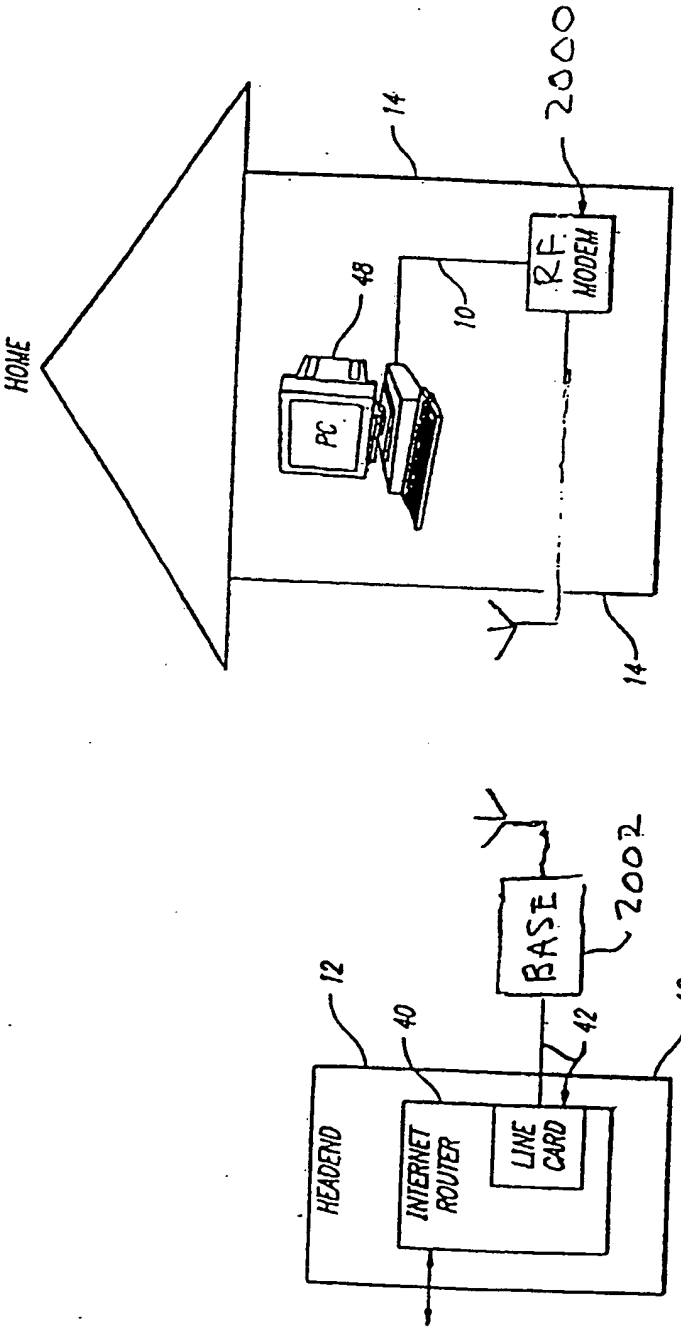


FIG. 21

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

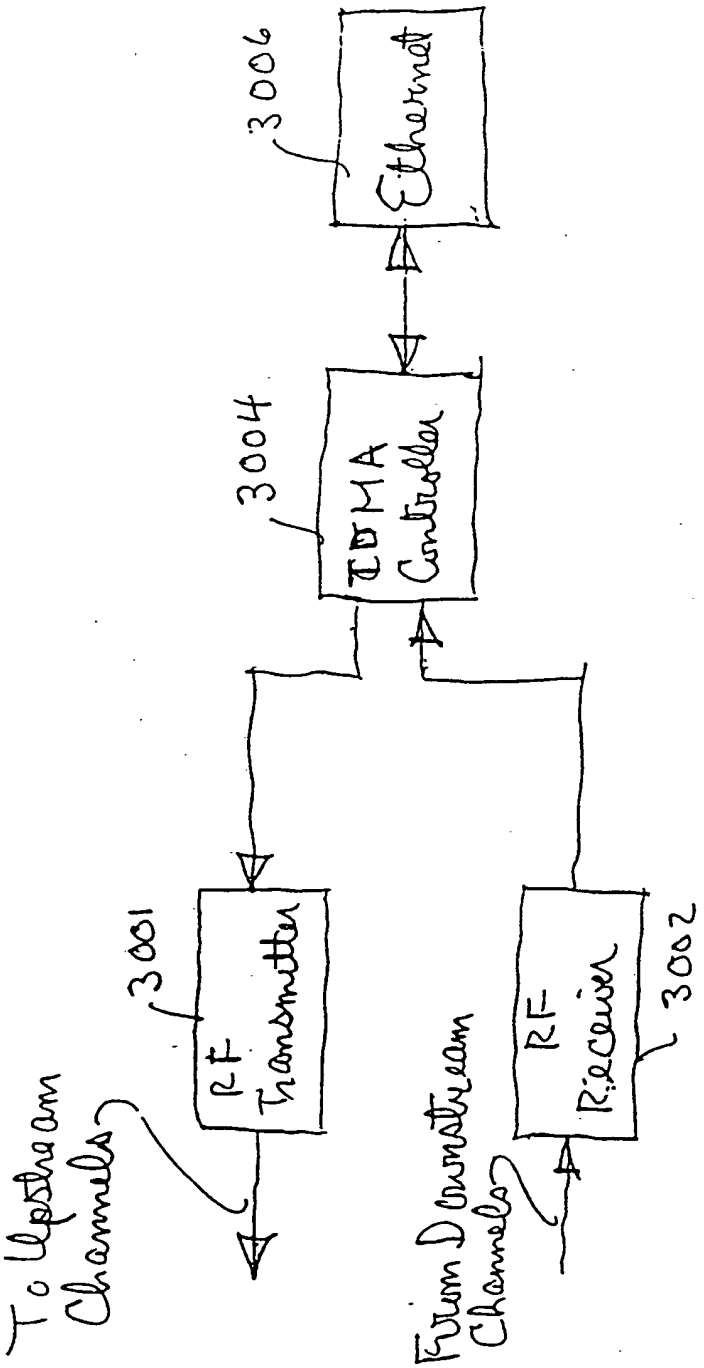


FIG. 22

DATA PACKET FRAGMENTATION IN A CABLE MODEM SYSTEM

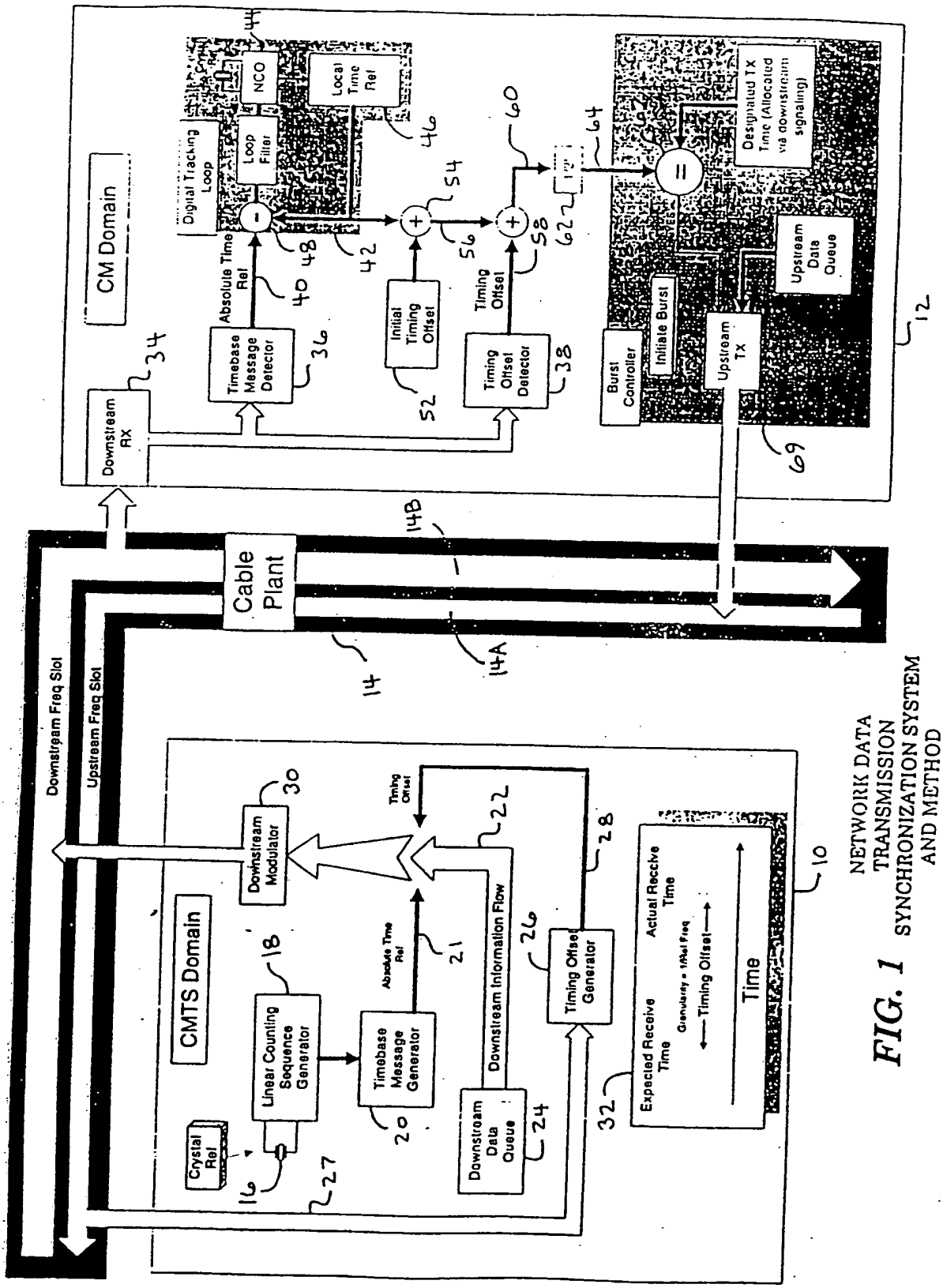


FIG. 1 NETWORK DATA TRANSMISSION SYNCHRONIZATION SYSTEM AND METHOD

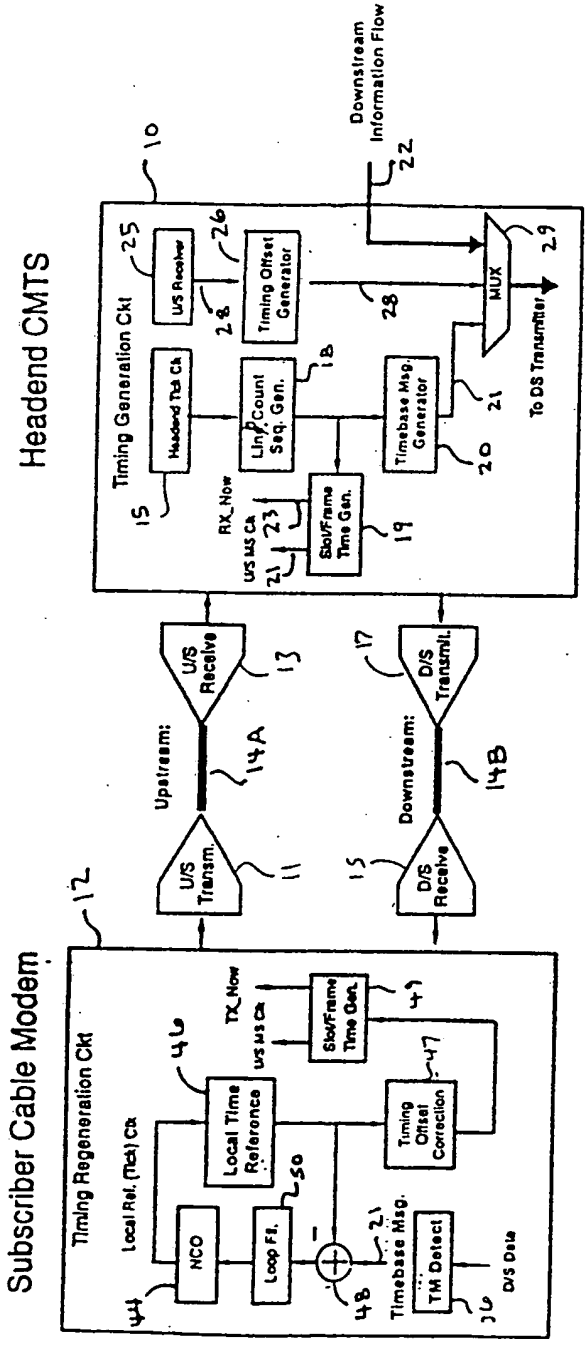
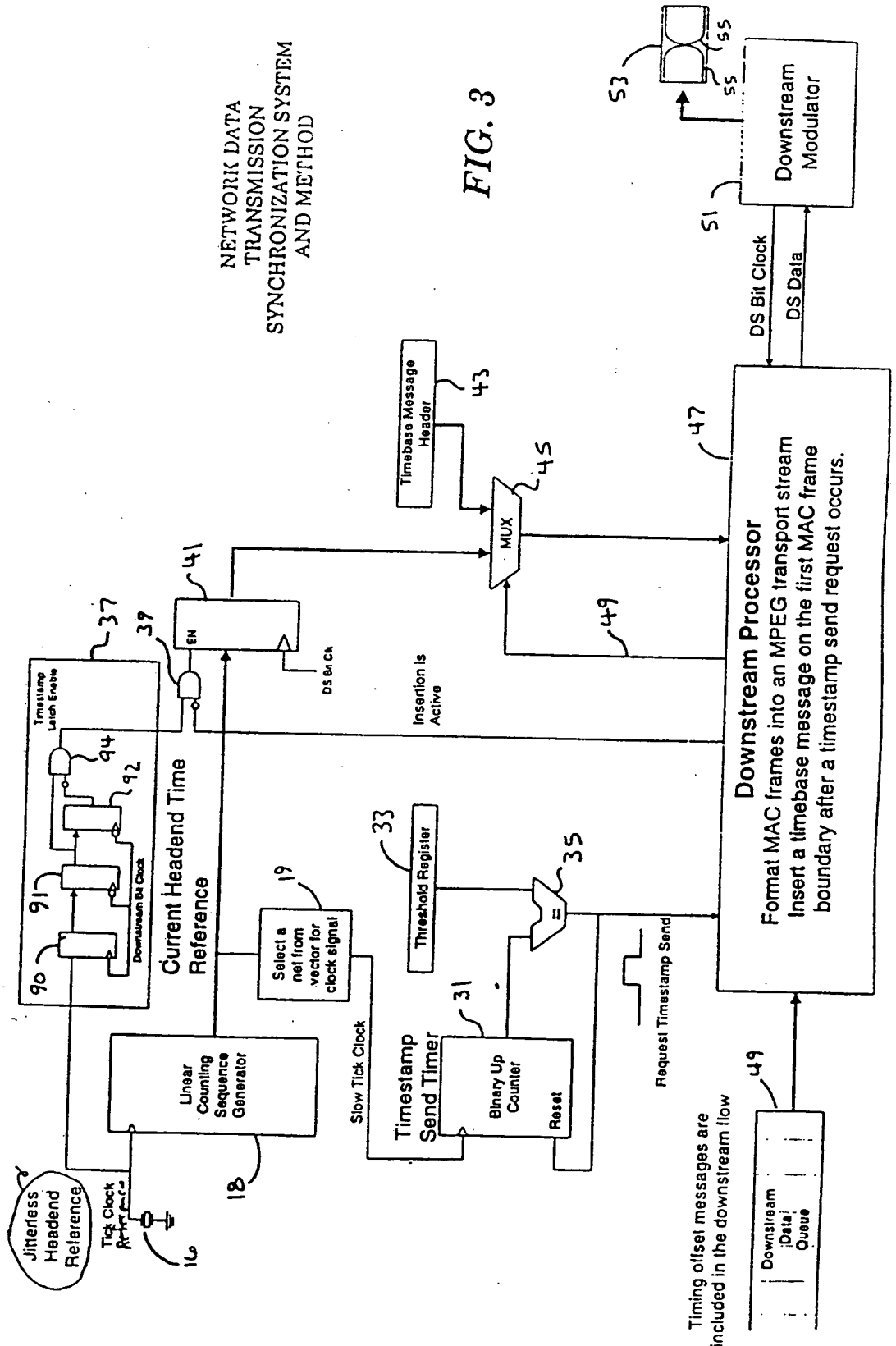


FIG. 2

NETWORK DATA TRANSMISSION SYNCHRONIZATION SYSTEM AND METHOD

NETWORK DATA TRANSMISSION SYNCHRONIZATION SYSTEM AND METHOD

FIG. 3



NETWORK DATA TRANSMISSION SYNCHRONIZATION SYSTEM AND METHOD

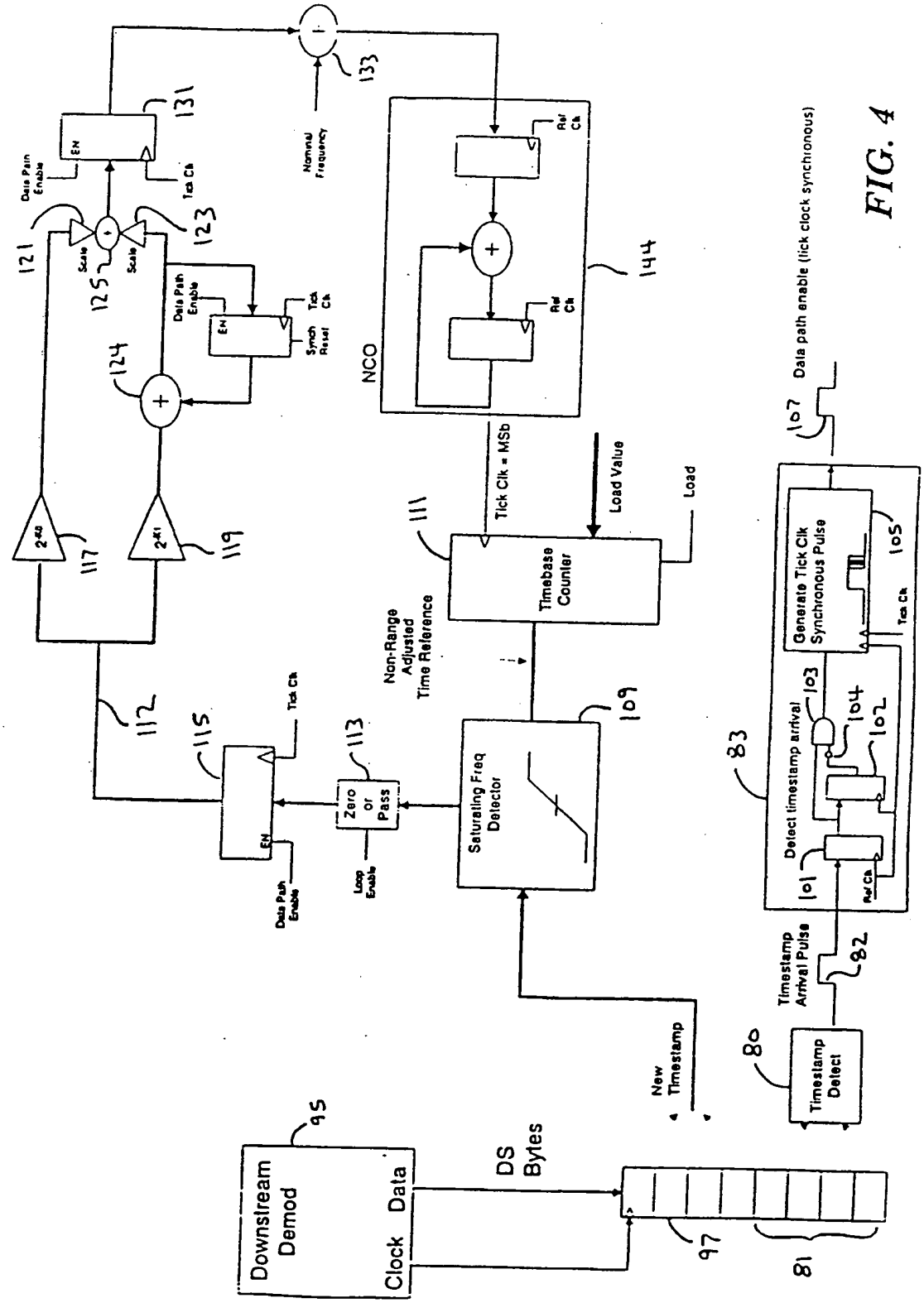


FIG. 4

Update Rate	Coarse Coeffs	Fine Coefficients
1kHz (1ms)	$K0 = 2^{-11}$ $K1 = 2^{-15}$ (BW=50Hz)	$K0 = 2^{-16}$ $K1 = 2^{-25}$ (BW=1Hz)
300Hz (3.3ms)	$K0 = 2^{-12}$ $K1 = 2^{-15}$ (BW=20Hz)	$K0 = 2^{-16}$ $K1 = 2^{-23}$ (BW=1Hz)
100Hz (10ms)	$K0 = 2^{-13}$ $K1 = 2^{-16}$ (BW=10Hz)	$K0 = 2^{-16}$ $K1 = 2^{-22}$ (BW=1Hz)
50Hz (20ms)	$K0 = 2^{-14}$ $K1 = 2^{-17}$ (BW=5Hz)	$K0 = 2^{-16}$ $K1 = 2^{-21}$ (BW=1Hz)
30Hz (33ms)	$K0 = 2^{-15}$ $K1 = 2^{-18}$ (BW=3Hz)	$K0 = 2^{-17}$ $K1 = 2^{-21}$ (BW=1Hz)
10Hz (100ms)	$K0 = 2^{-17}$ $K1 = 2^{-20}$ (BW=1Hz)	$K0 = 2^{-17}$ $K1 = 2^{-20}$ (BW=1Hz)
5Hz (200ms)	$K0 = 2^{-18}$ $K1 = 2^{-20}$ (BW=1Hz)	$K0 = 2^{-18}$ $K1 = 2^{-20}$ (BW=1Hz)

FIG. 5

NETWORK DATA
TRANSMISSION
SYNCHRONIZATION SYSTEM
AND METHOD

NETWORK DATA
TRANSMISSION
SYNCHRONIZATION SYSTEM
AND METHOD

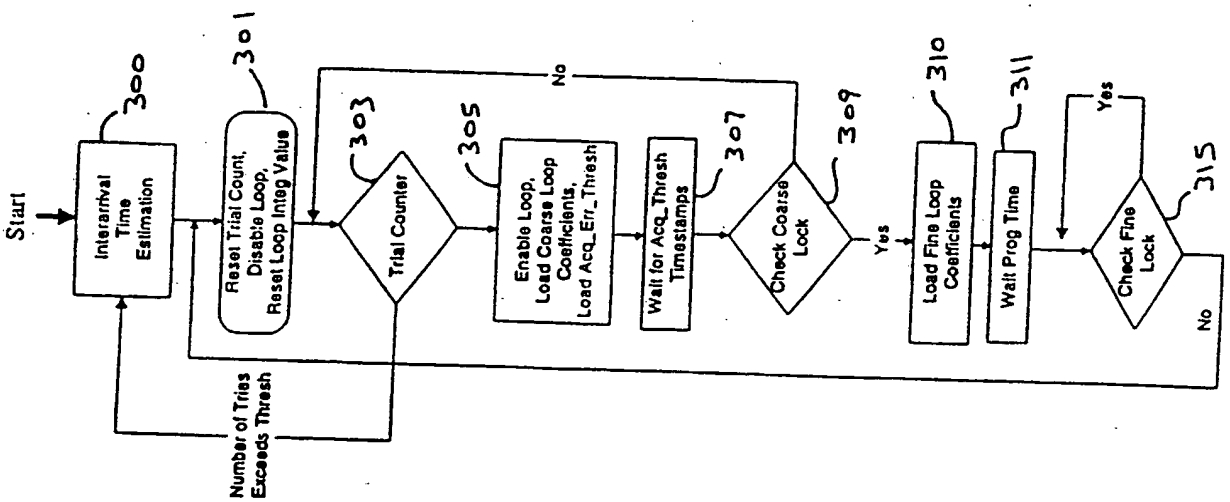


FIG. 6

NETWORK DATA TRANSMISSION SYNCHRONIZATION SYSTEM AND METHOD

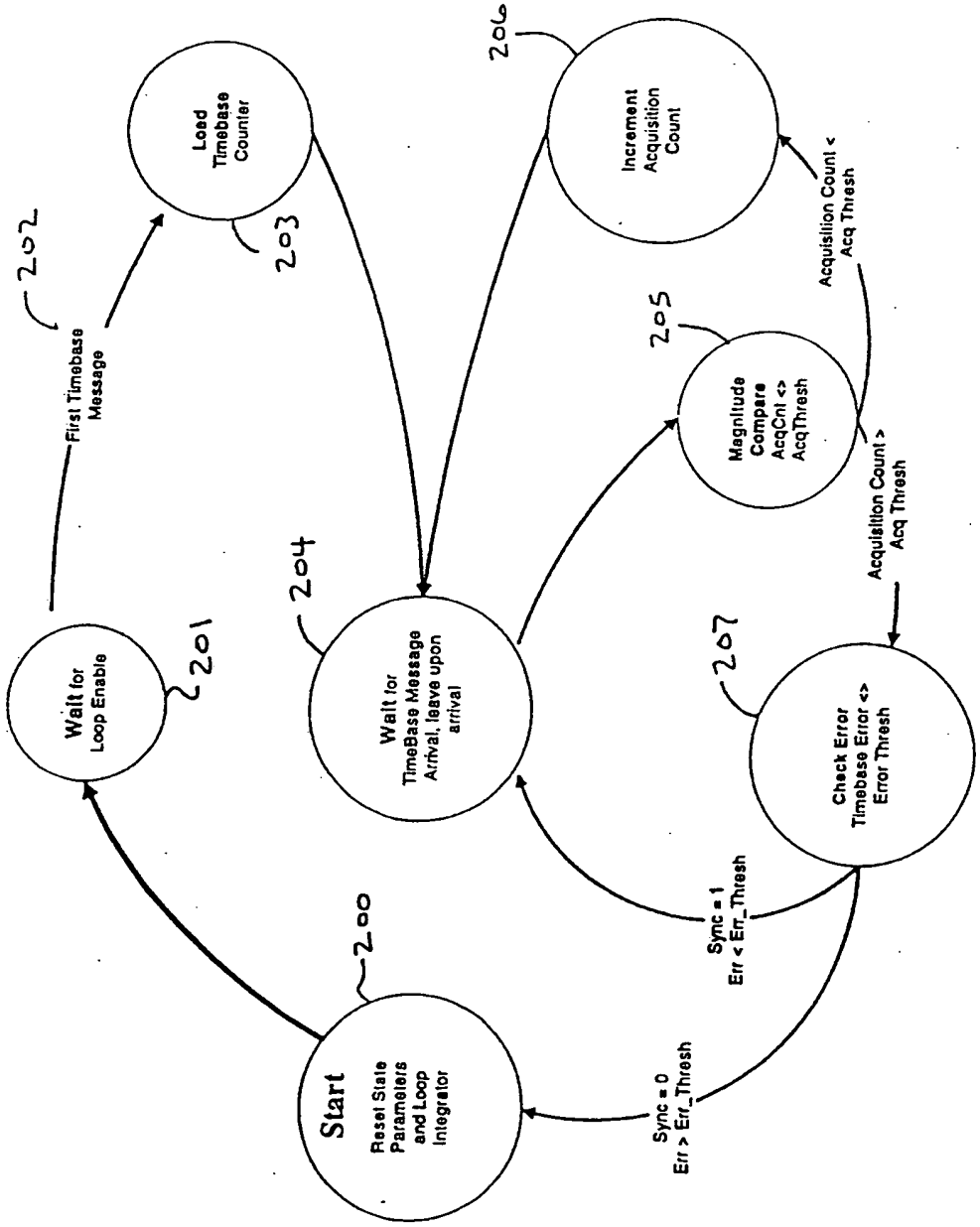


FIG. 7

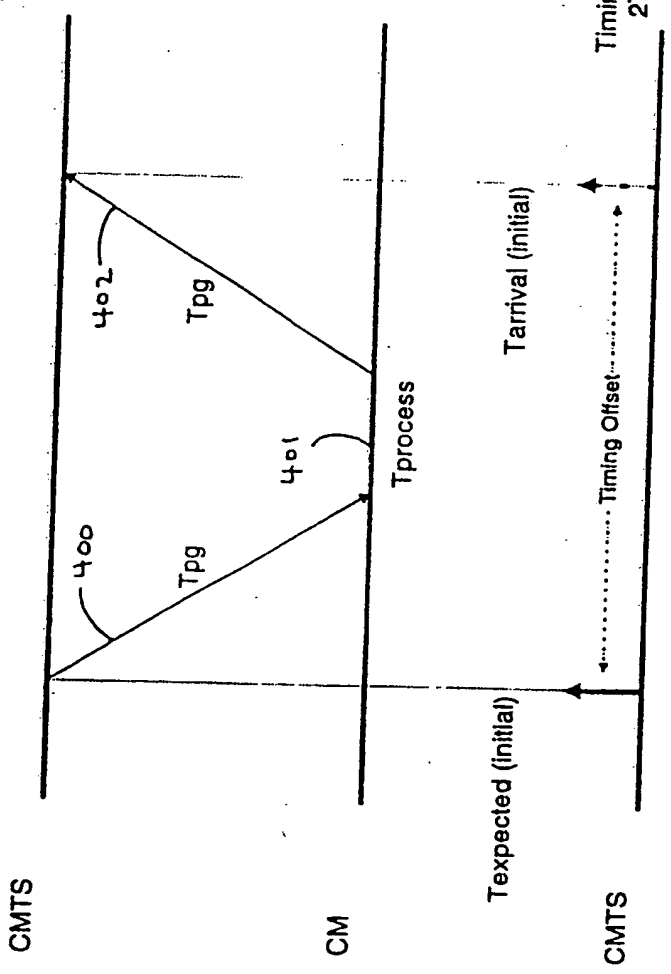


FIG. 8

NETWORK DATA
TRANSMISSION
SYNCHRONIZATION SYSTEM
AND METHOD

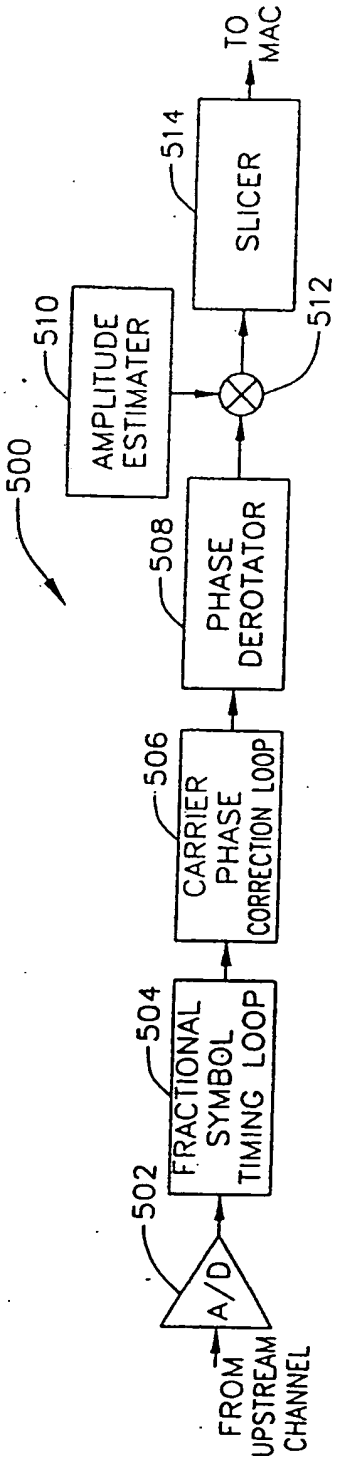


FIG. 1

BURST RECEIVER FOR CABLE MODEM SYSTEM

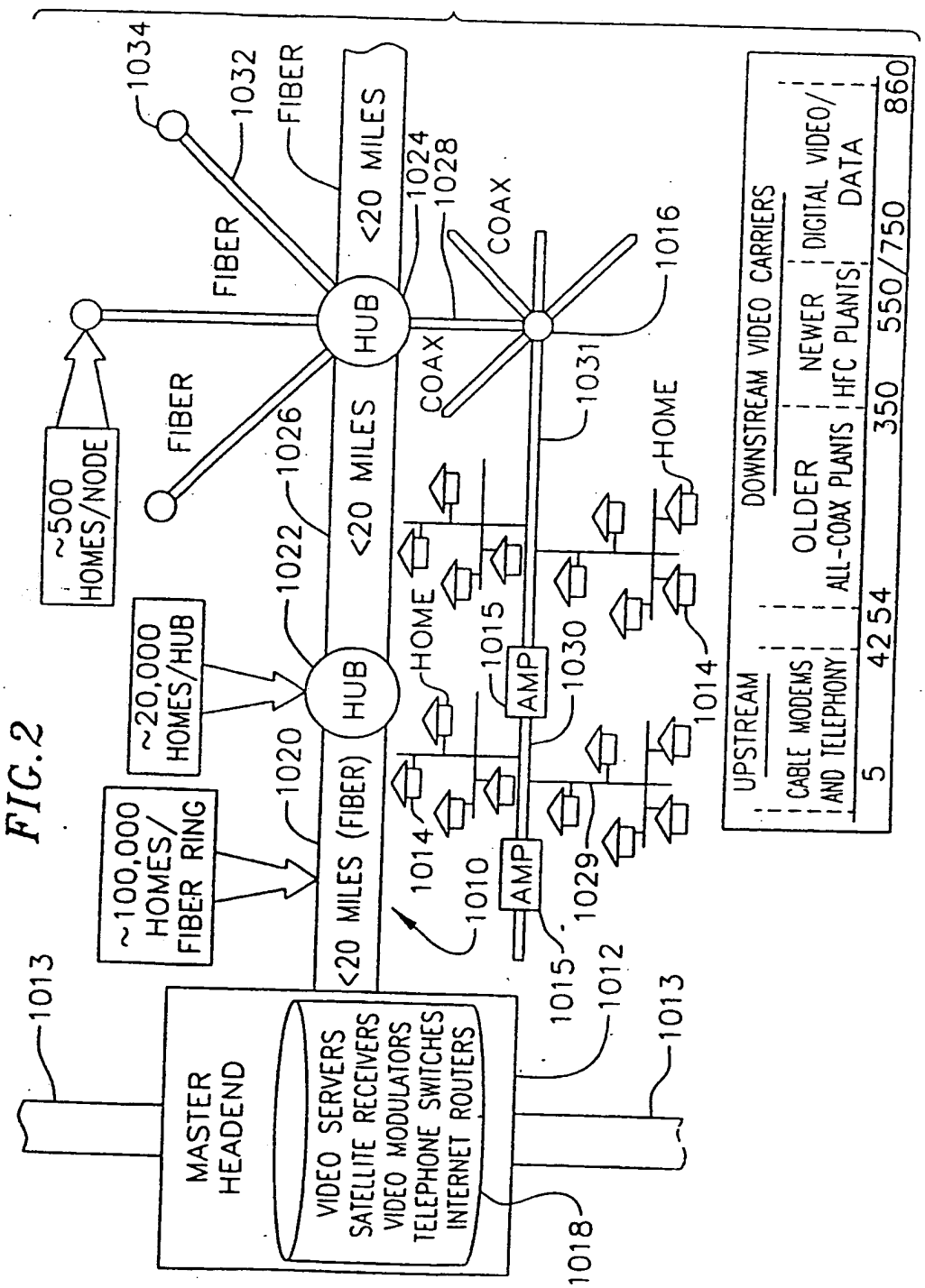


FIG. 2

BURST RECEIVER FOR CABLE MODEM SYSTEM

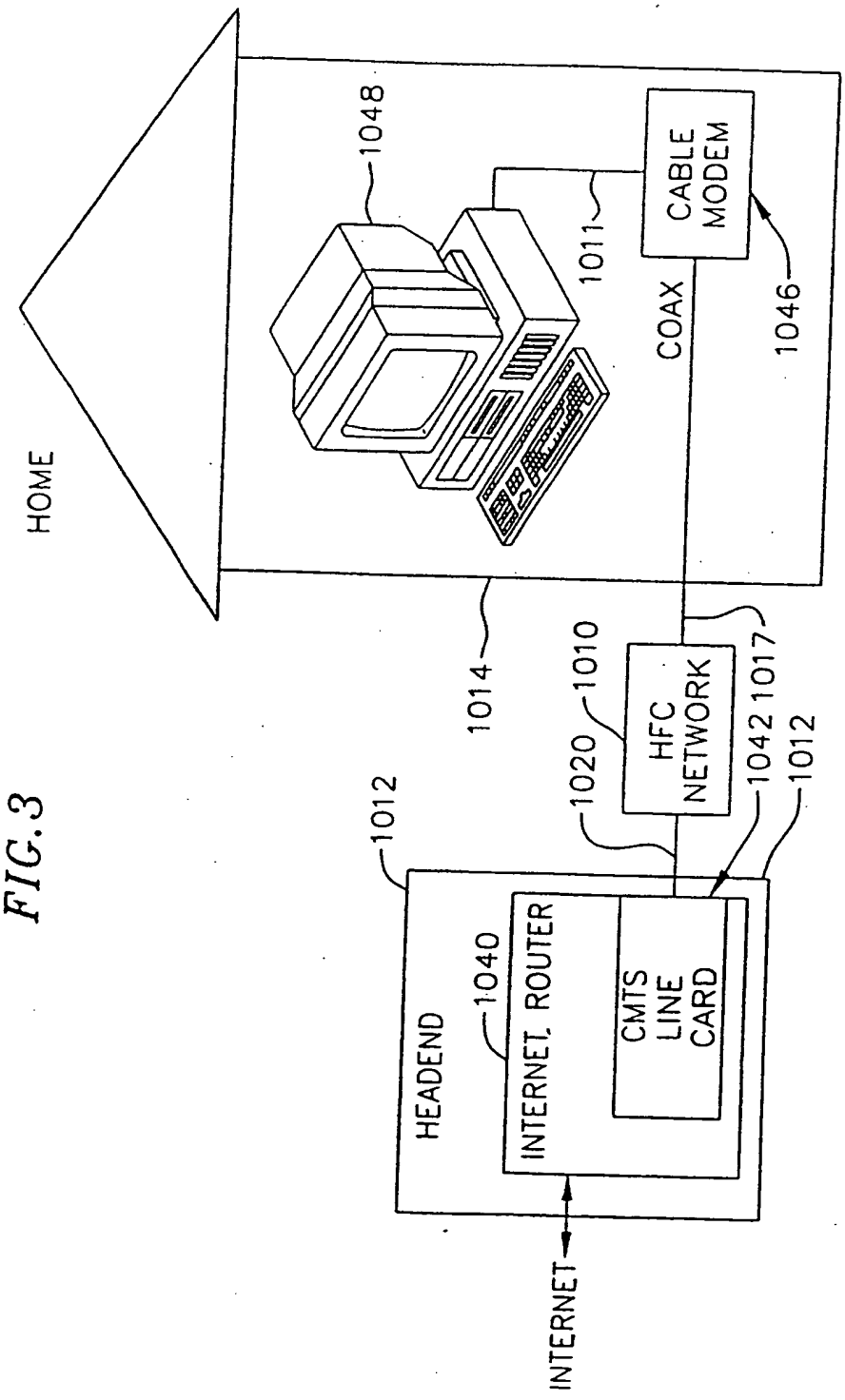


FIG. 3

BURST RECEIVER FOR CABLE MODEM SYSTEM

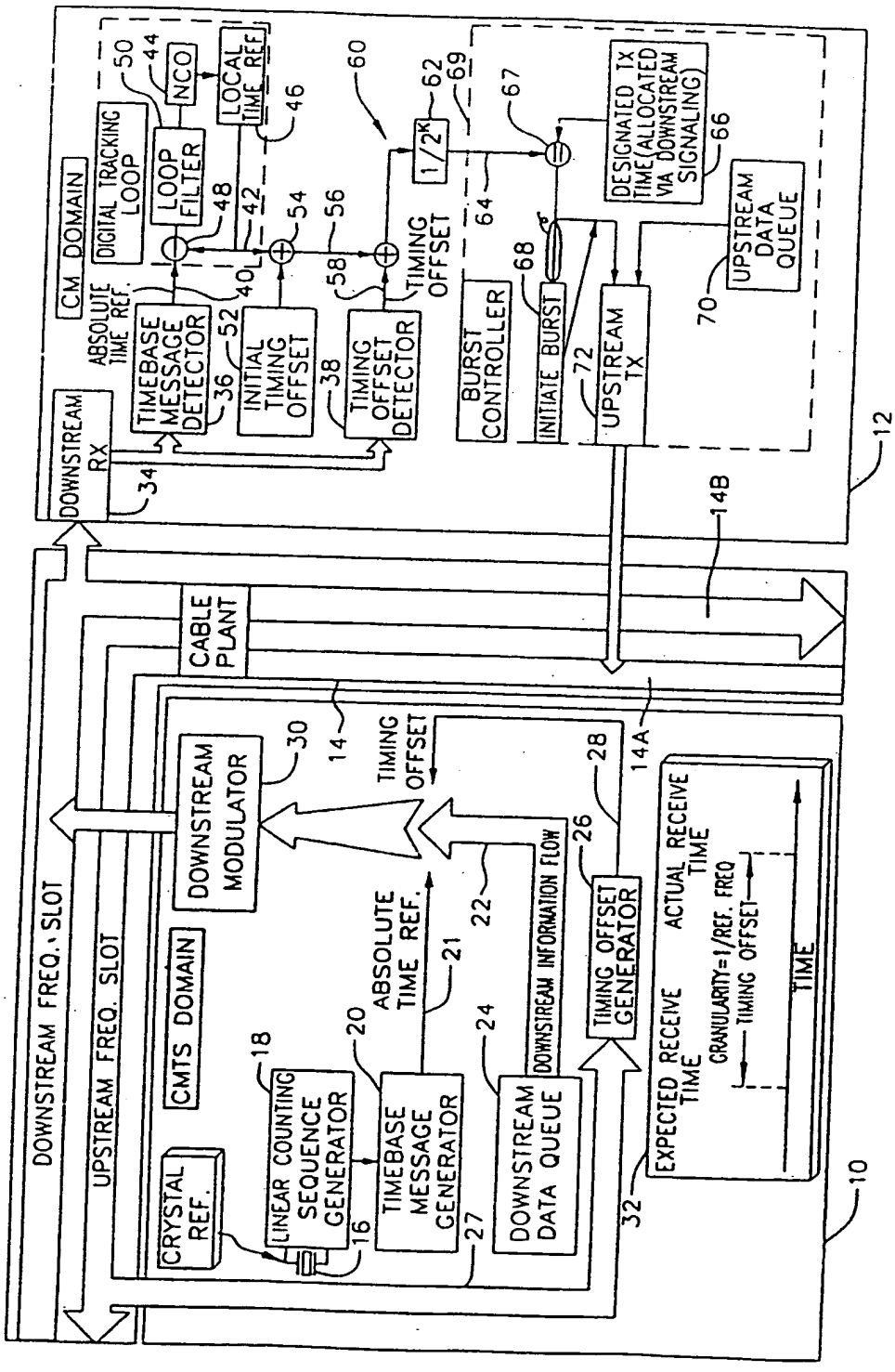
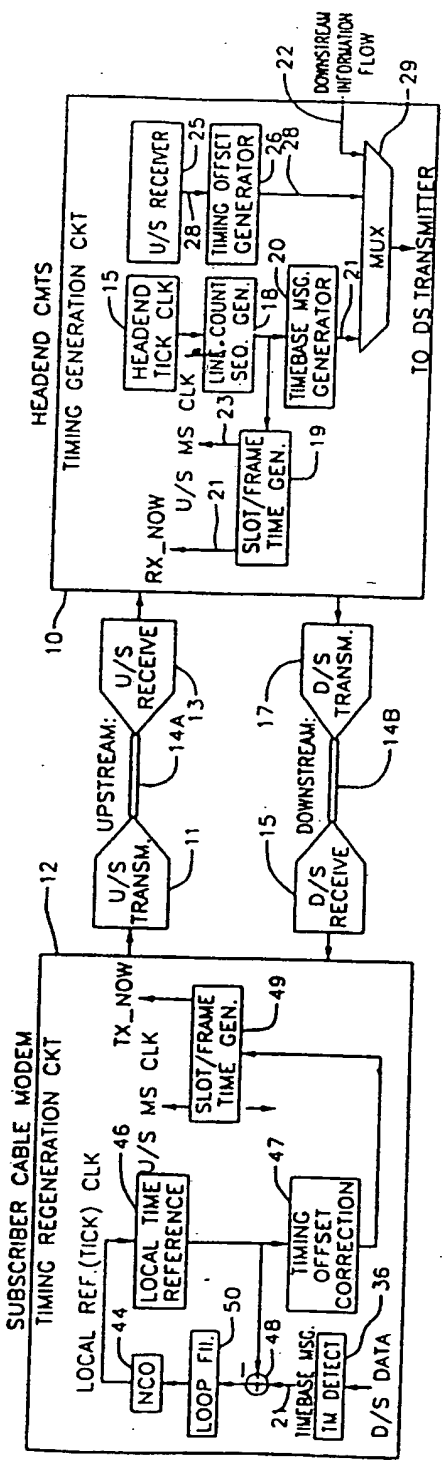


FIG. 4

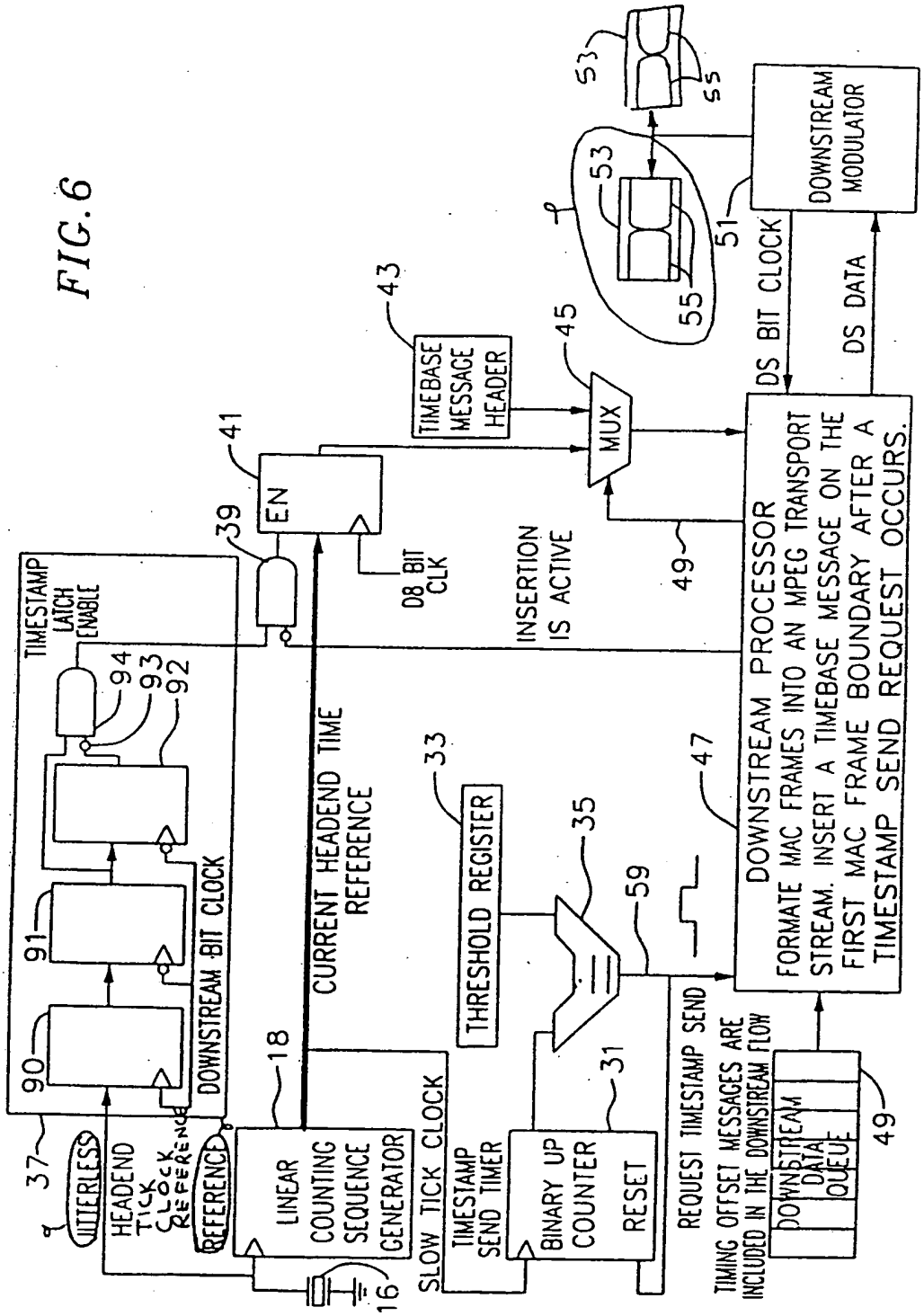
BURST RECEIVER FOR CABLE MODEM SYSTEM

FIG.5



BURST RECEIVER FOR CABLE MODEM SYSTEM

FIG. 6



BURST RECEIVER FOR CABLE MODEM SYSTEM

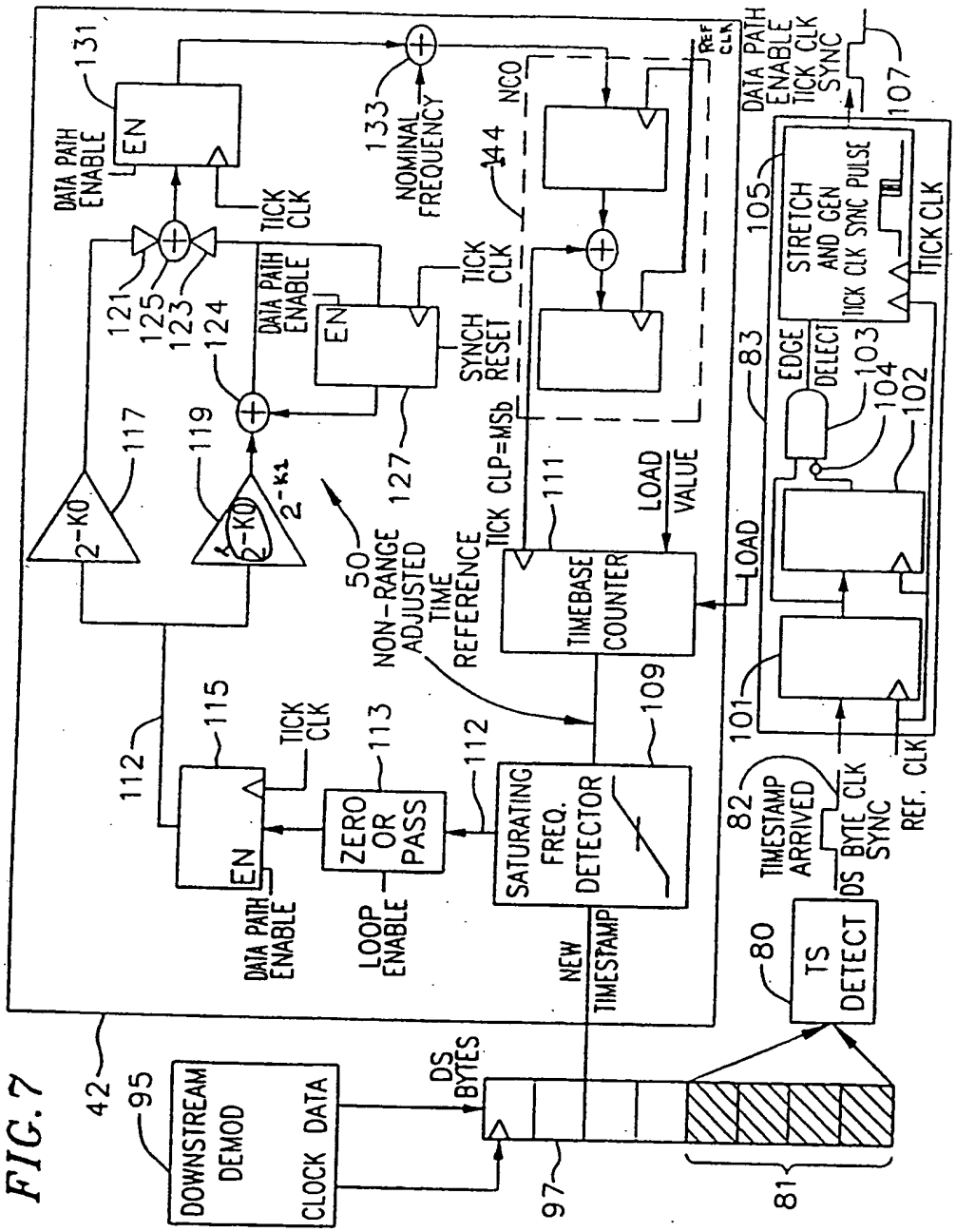


FIG. 7

BURST RECEIVER FOR CABLE MODEM SYSTEM

FIG.8

UPDATE RATE	COARSE COEFFS	FINE COEFFICIENTS
1kHz(1ms)	$K0=2^{-11}$ $K1=2^{-15}$ (BW=50Hz)	$K0=2^{-16}$ $K1=2^{-25}$ (BW=1Hz)
300Hz(3.3ms)	$K0=2^{-12}$ $K1=2^{-15}$ (BW=20Hz)	$K0=2^{-16}$ $K1=2^{-23}$ (BW=1Hz)
100Hz(10ms)	$K0=2^{-13}$ $K1=2^{-16}$ (BW=10Hz)	$K0=2^{-16}$ $K1=2^{-22}$ (BW=1Hz)
50Hz(20ms)	$K0=2^{-14}$ $K1=2^{-17}$ (BW=5Hz)	$K0=2^{-16}$ $K1=2^{-21}$ (BW=1Hz)
30Hz(33ms)	$K0=2^{-15}$ $K1=2^{-18}$ (BW=3Hz)	$K0=2^{-17}$ $K1=2^{-21}$ (BW=1Hz)
10Hz(100ms)	$K0=2^{-17}$ $K1=2^{-20}$ (BW=1Hz)	$K0=2^{-17}$ $K1=2^{-20}$ (BW=1Hz)
5Hz(200ms)	$K0=2^{-18}$ $K1=2^{-20}$ (BW=1Hz)	$K0=2^{-18}$ $K1=2^{-20}$ (BW=1Hz)

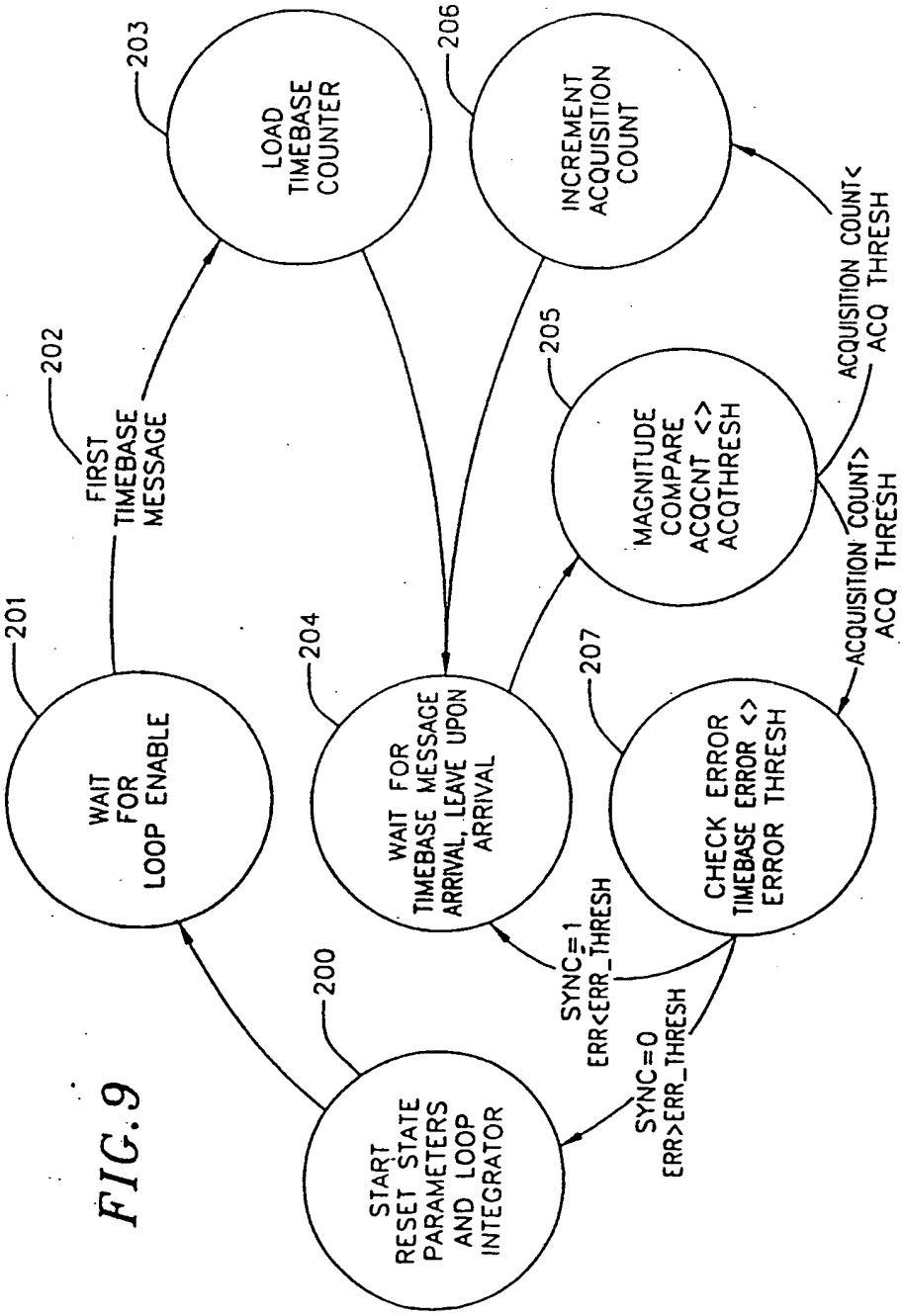


FIG. 9

BURST RECEIVER FOR
CABLE MODEM SYSTEM

FIG. 10

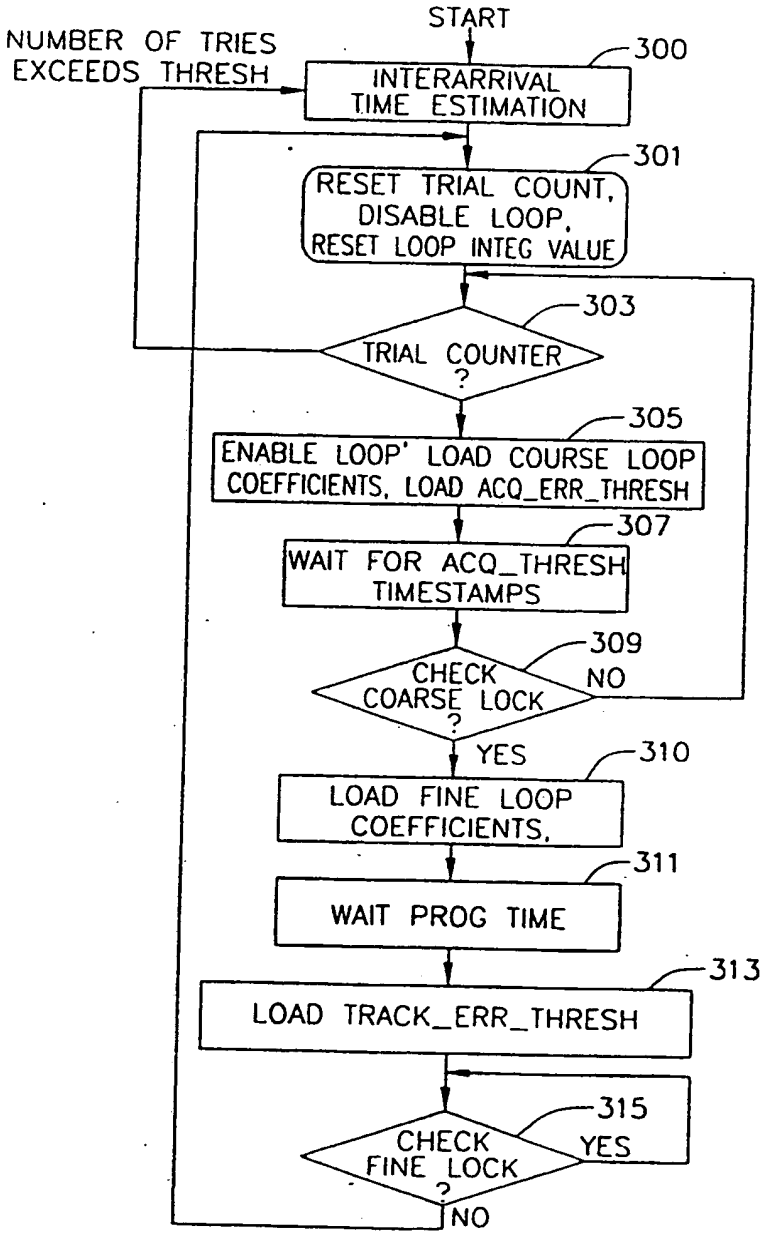
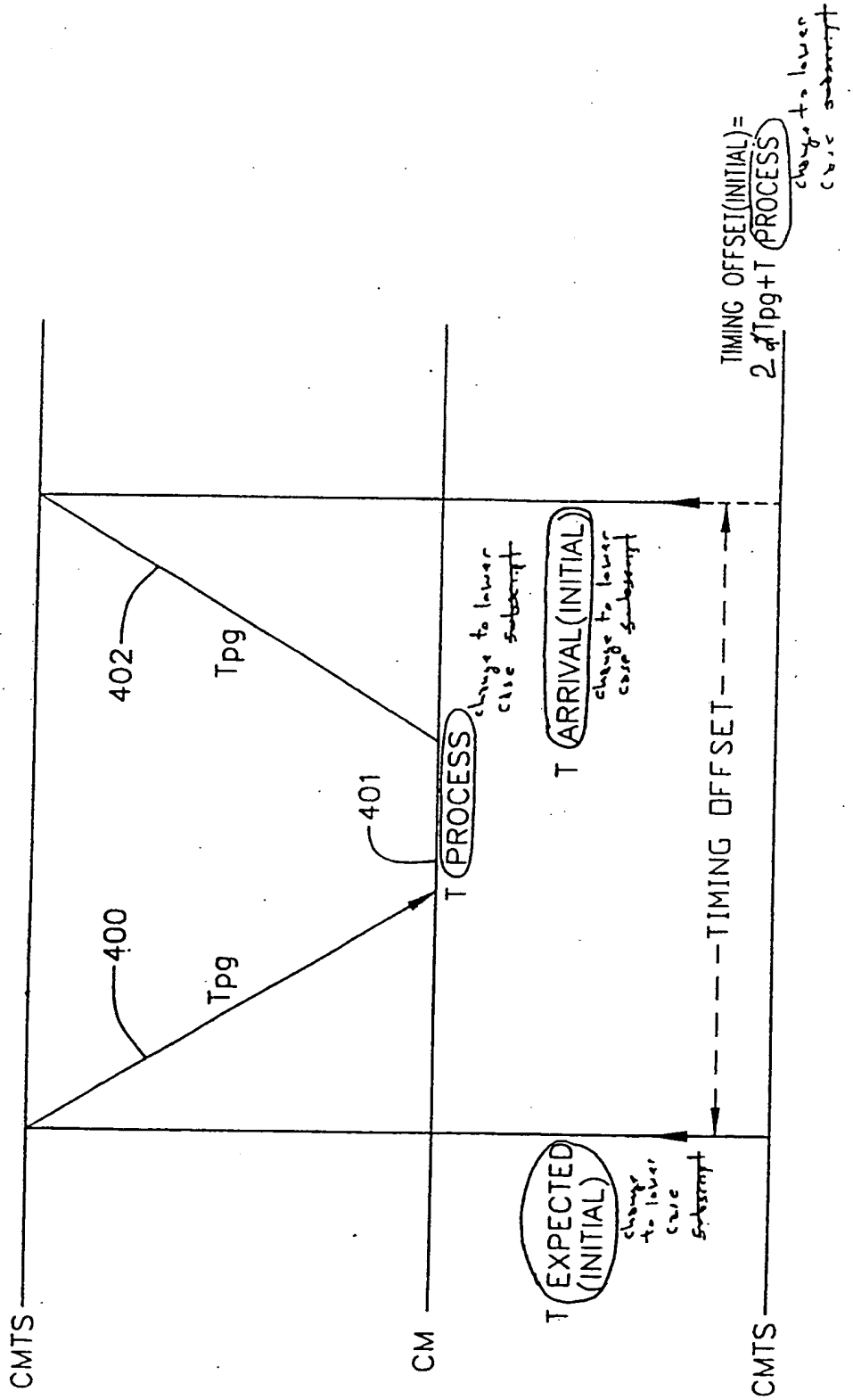

START
NUMBER OF TRIES EXCEEDS THRESH
300
INTERARRIVAL TIME ESTIMATION
301
RESET TRIAL COUNT, DISABLE LOOP, RESET LOOP INTEG VALUE
303
TRIAL COUNTER ?
305
ENABLE LOOP' LOAD COURSE LOOP COEFFICIENTS, LOAD ACQ_ERR_THRESH
307
WAIT FOR ACQ_THRESH TIMESTAMPS
309
CHECK COARSE LOCK ?
NO
YES
310
LOAD FINE LOOP COEFFICIENTS,
311
WAIT PROG TIME
313
LOAD TRACK_ERR_THRESH
315
CHECK FINE LOCK ?
YES
NO

FIG. 11



BURST RECEIVER FOR CABLE MODEM SYSTEM

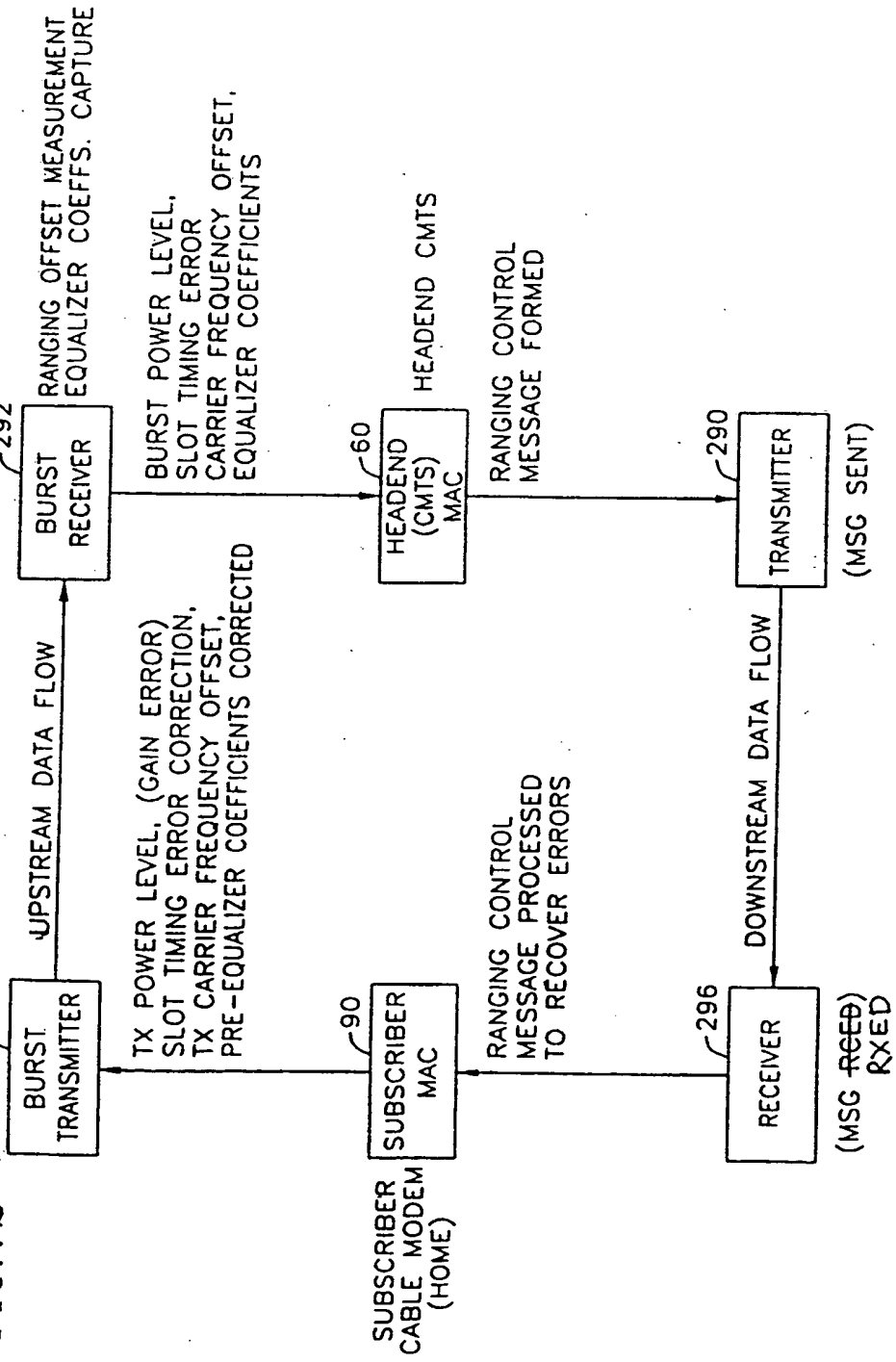
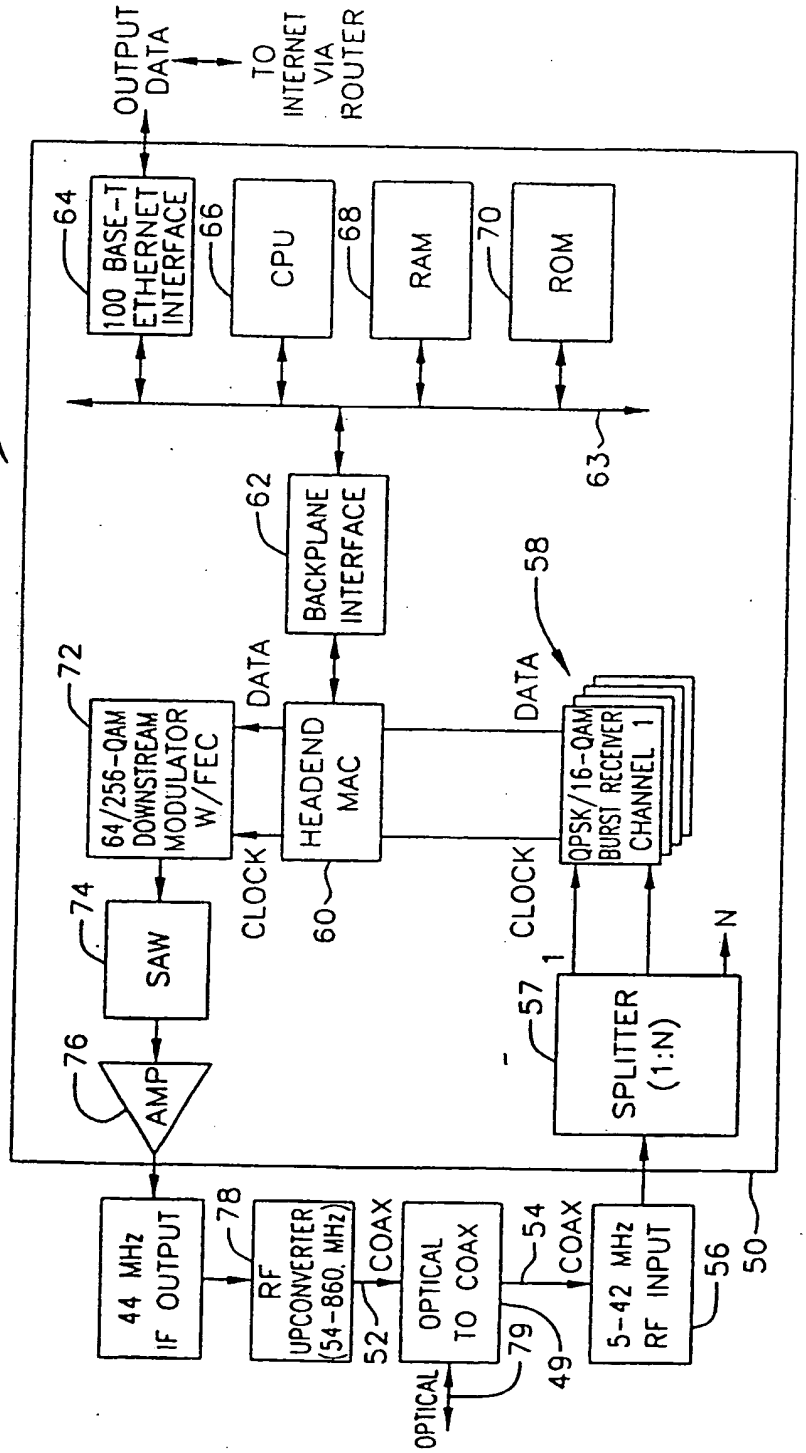

BURST RECEIVER FOR CABLE MODEM SYSTEM
SUBSCRIBER CABLE MODEM (HOME)
294
BURST TRANSMITTER
UPSTREAM DATA FLOW
292
BURST RECEIVER
RANGING OFFSET MEASUREMENT EQUALIZER COEFFS. CAPTURE
TX POWER LEVEL, (GAIN ERROR) SLOT TIMING ERROR CORRECTION, TX CARRIER FREQUENCY OFFSET, PRE-EQUALIZER COEFFICIENTS CORRECTED
BURST POWER LEVEL, SLOT TIMING ERROR CARRIER FREQUENCY OFFSET, EQUALIZER COEFFICIENTS
90
SUBSCRIBER MAC
60
HEADEND (CMTS) MAC
HEADEND CMTS
RANGING CONTROL MESSAGE PROCESSED TO RECOVER ERRORS
RANGING CONTROL MESSAGE FORMED
296
RECEIVER
DOWNSTREAM DATA FLOW
290
TRANSMITTER
(MSG RCED) RXED
(MSG SENT)

FIG. 12

FIG. 13



BURST RECEIVER FOR CABLE MODEM SYSTEM

FIG. 14

PRIOR ART

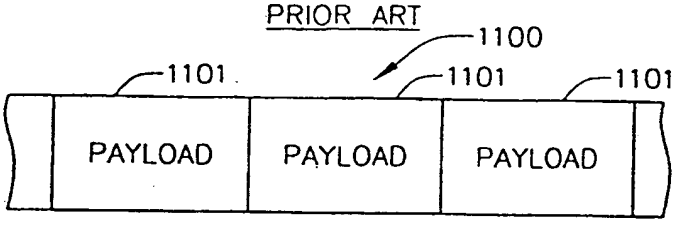


FIG. 15

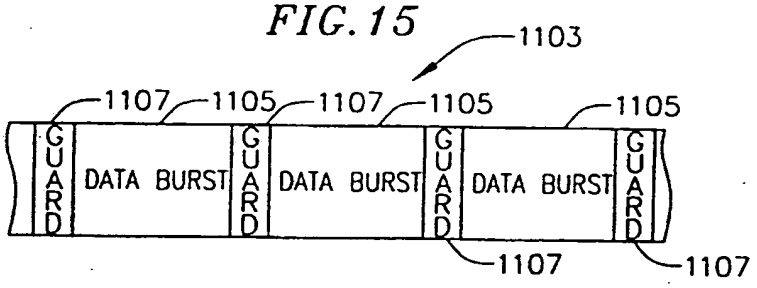


FIG. 16

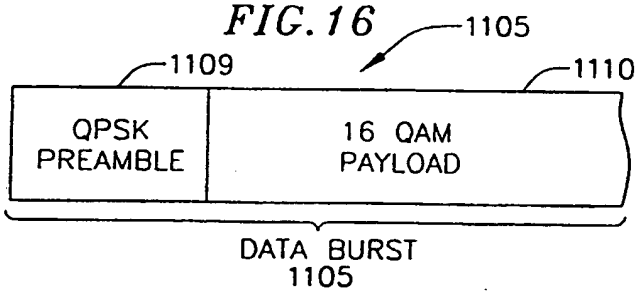
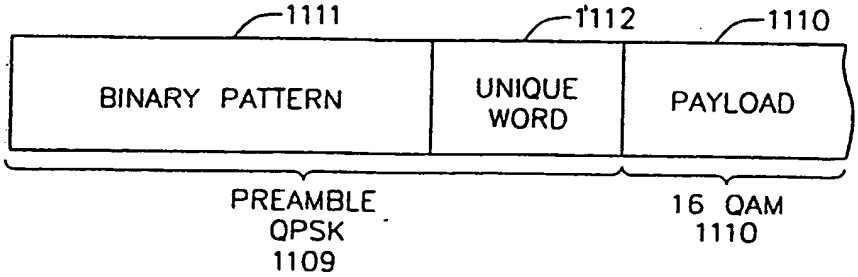


FIG. 17



BURST RECEIVER FOR CABLE MODEM SYSTEM

FIG. 18
PRIOR ART

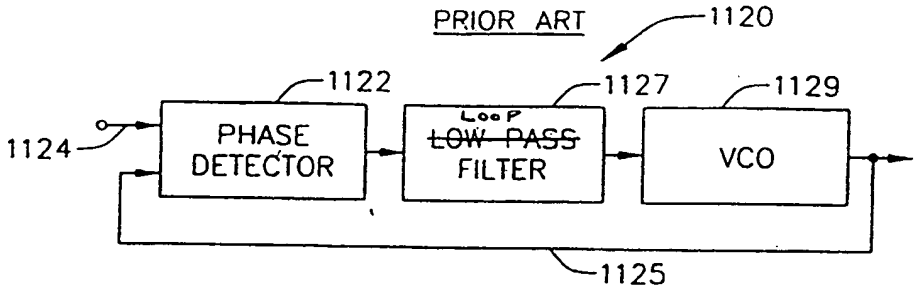


FIG. 19

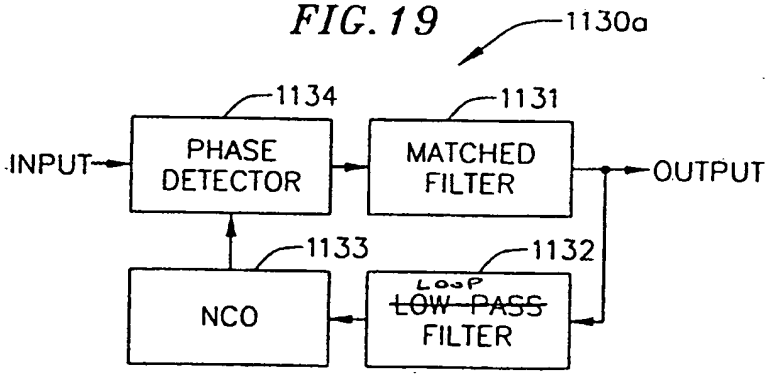


FIG. 20

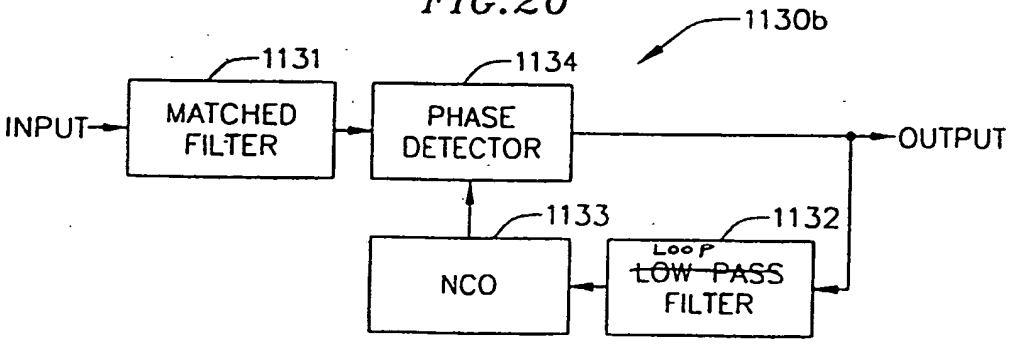
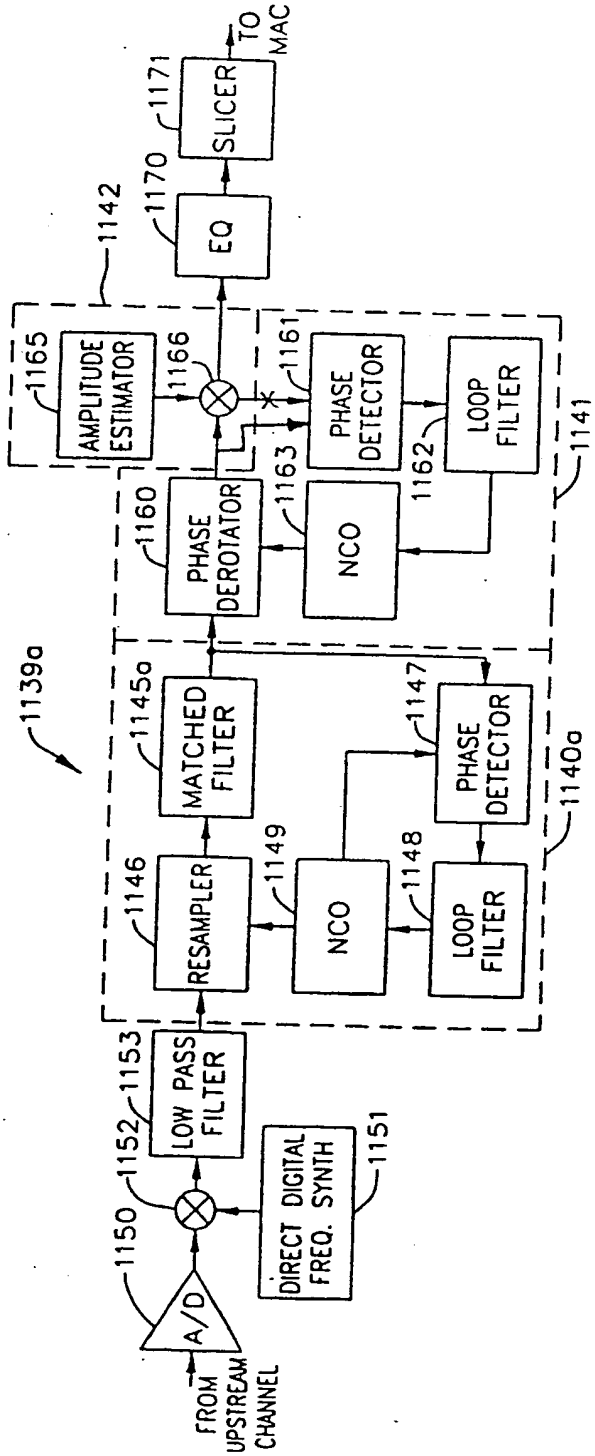


FIG.21



BURST RECEIVER FOR CABLE MODEM SYSTEM

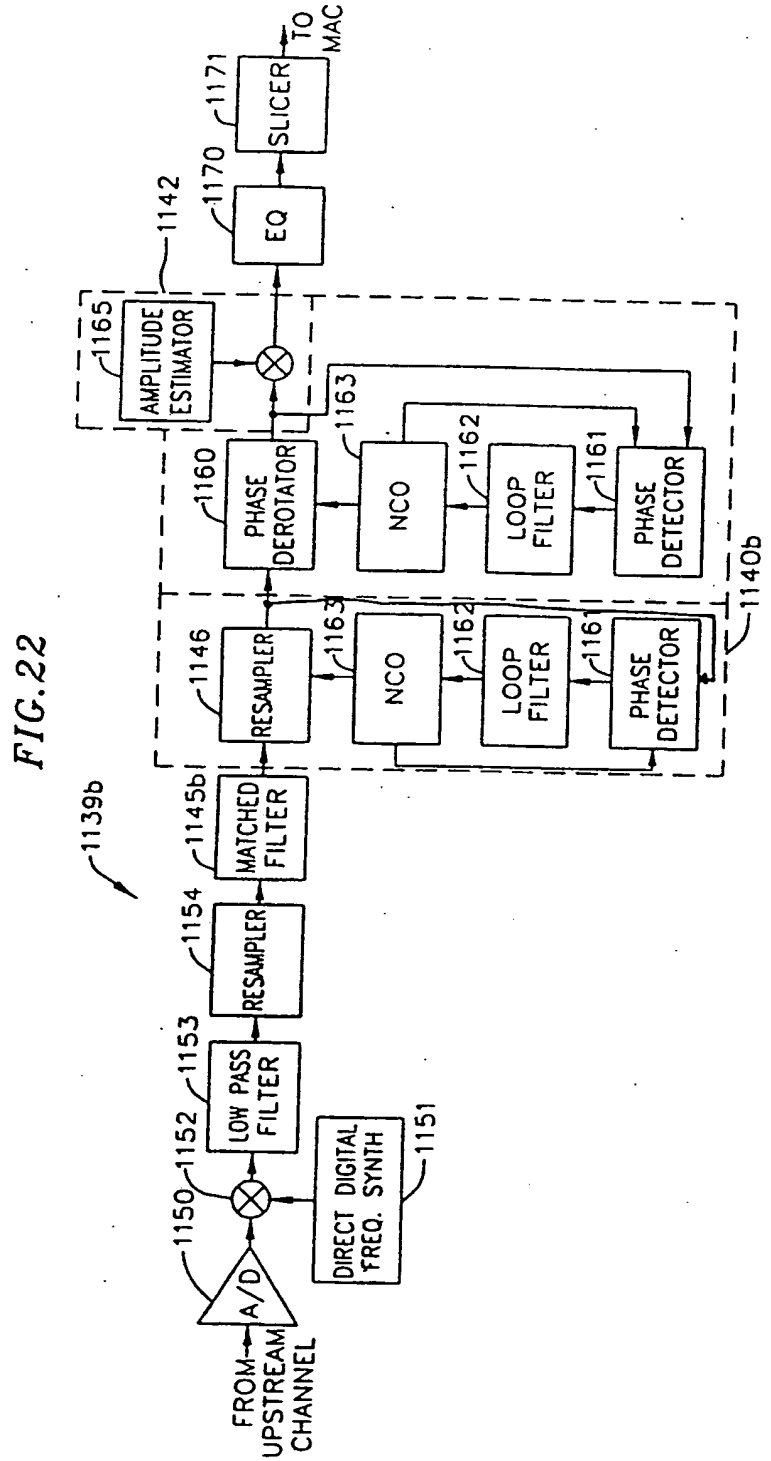


FIG.22

BURST RECEIVER FOR CABLE MODEM SYSTEM

FIG.23

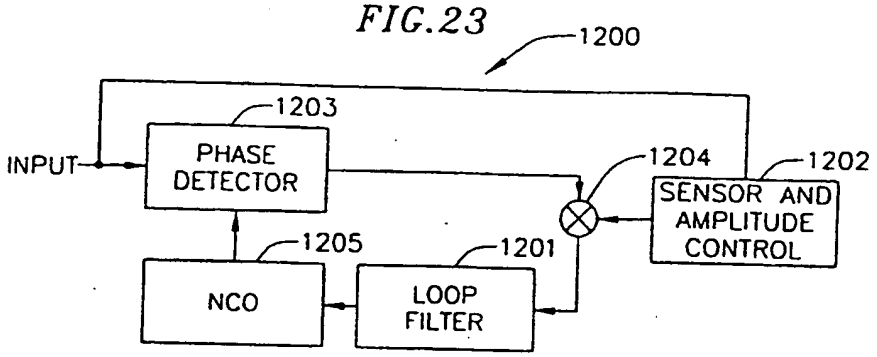


FIG.24

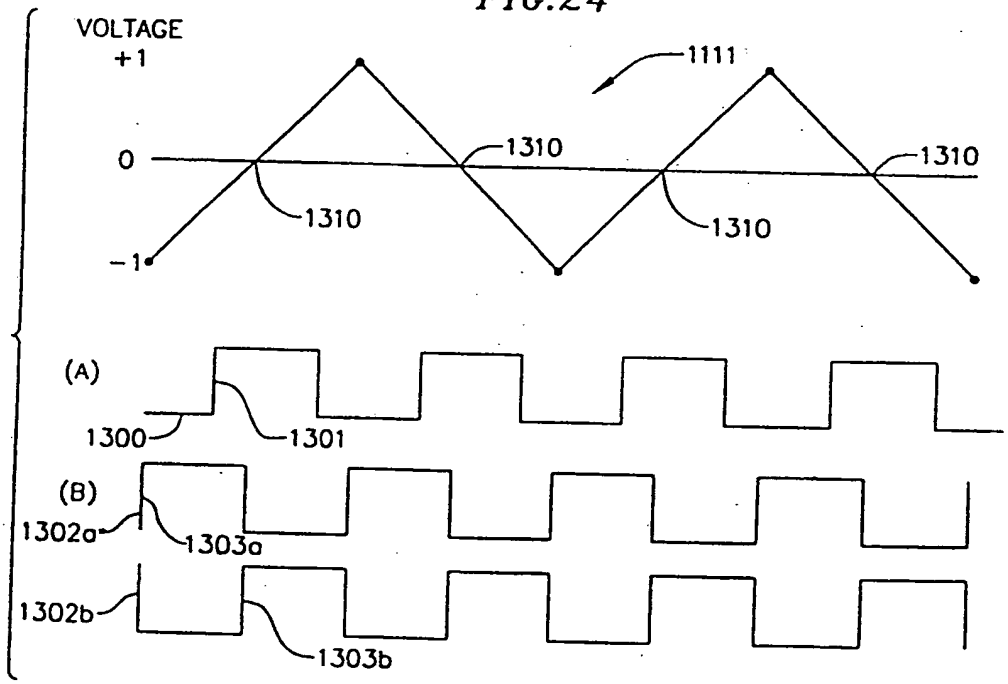


FIG.25

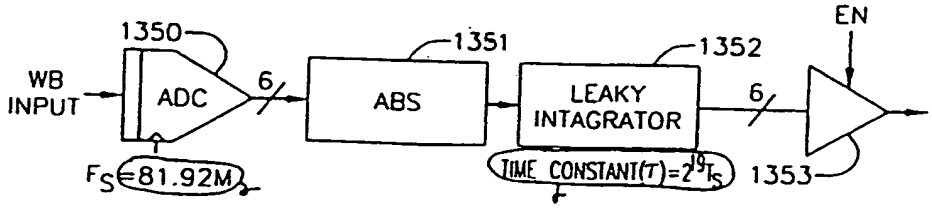
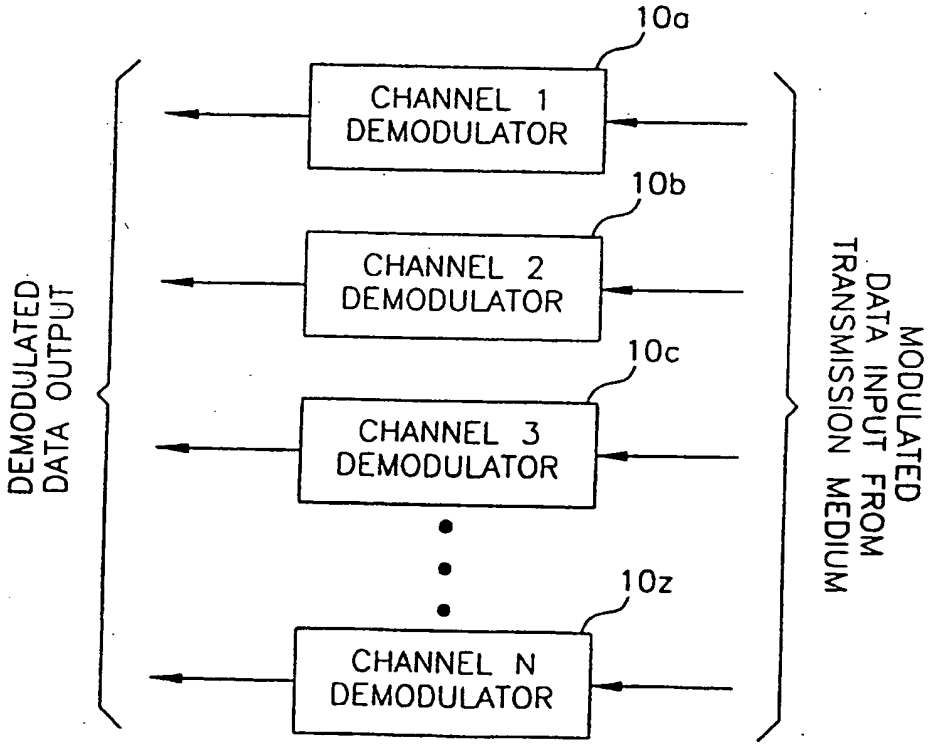


FIG. 1
PRIOR ART



ROBUST TECHNIQUES FOR
OPTIMAL UPSTREAM
COMMUNICATION

FIG. 2

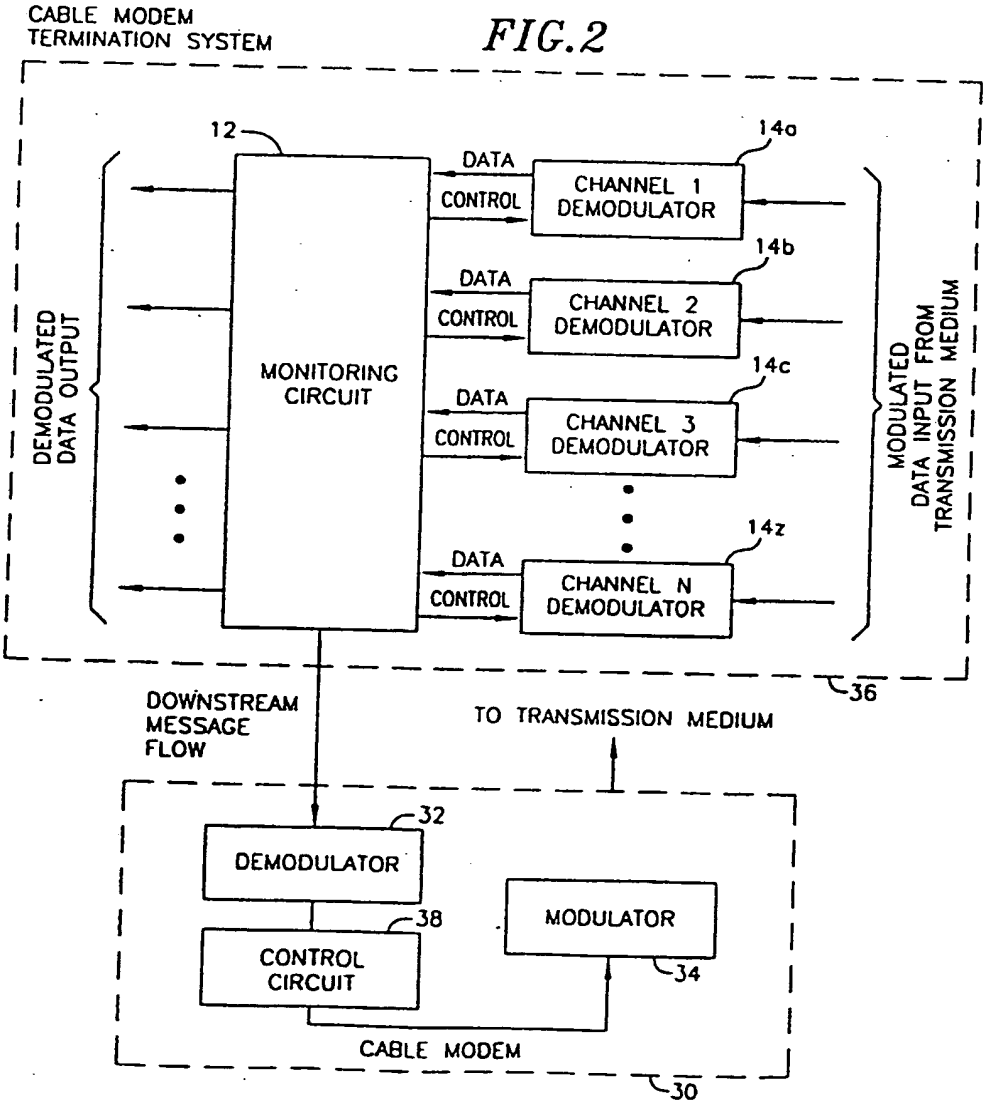
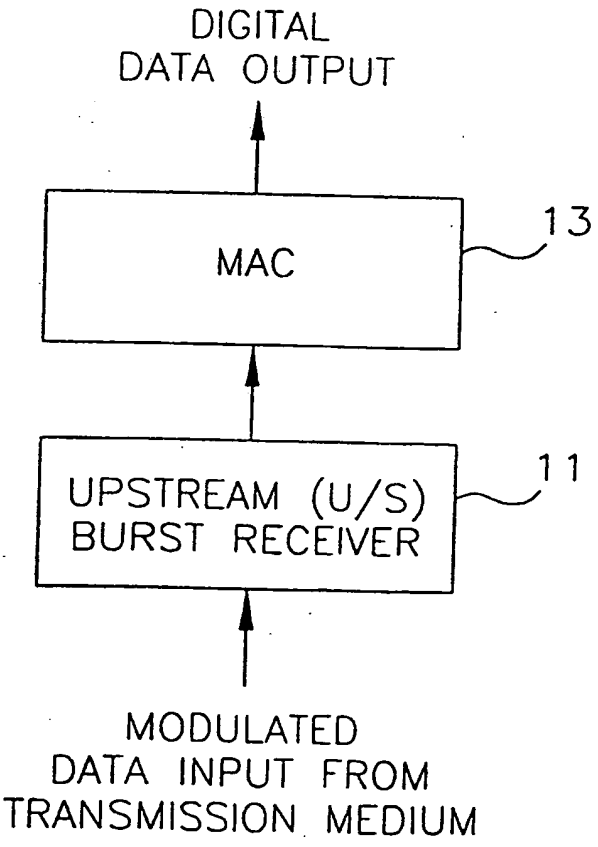


FIG.3
PRIOR ART



ROBUST TECHNIQUES FOR
OPTIMAL UPSTREAM
COMMUNICATION

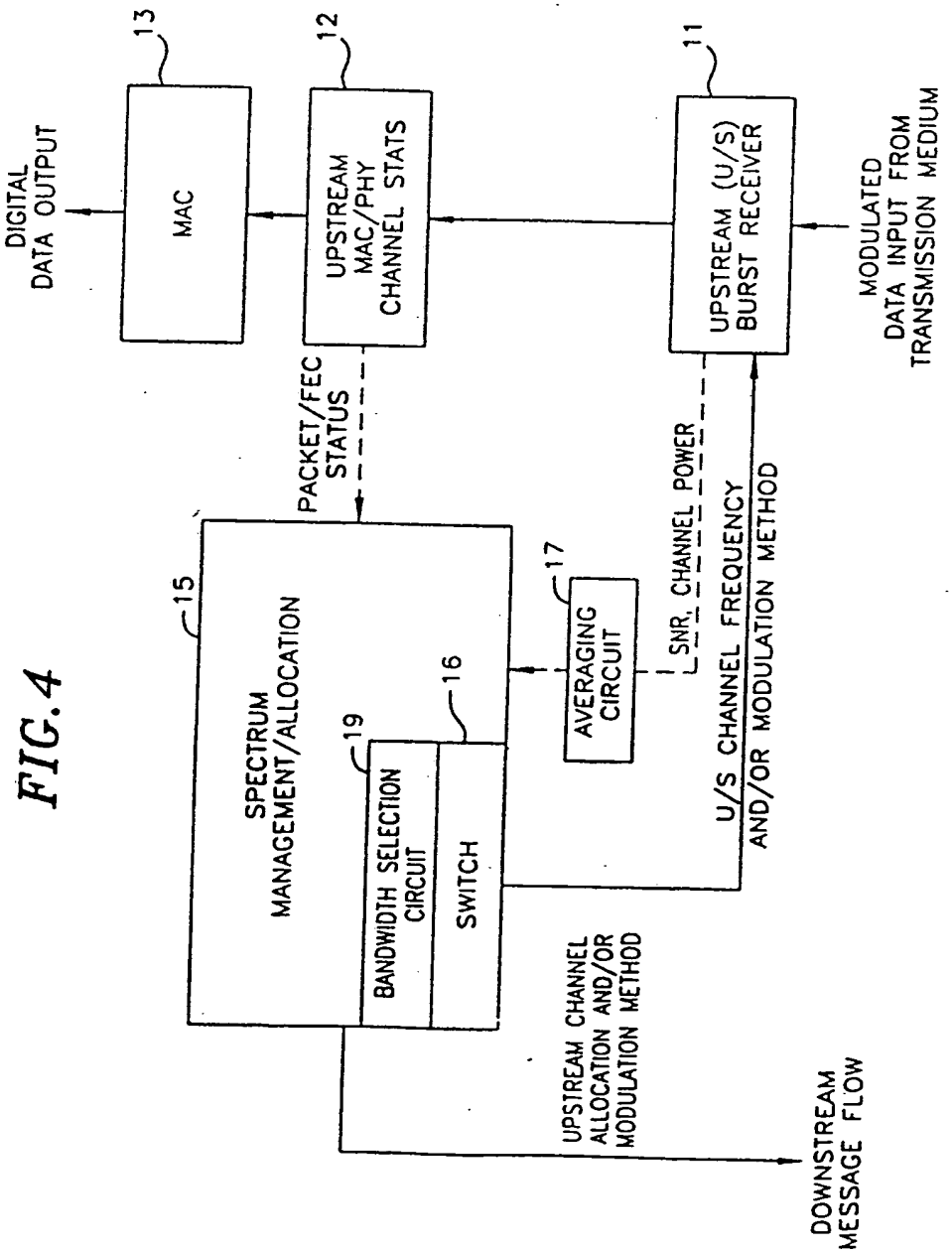


FIG. 4

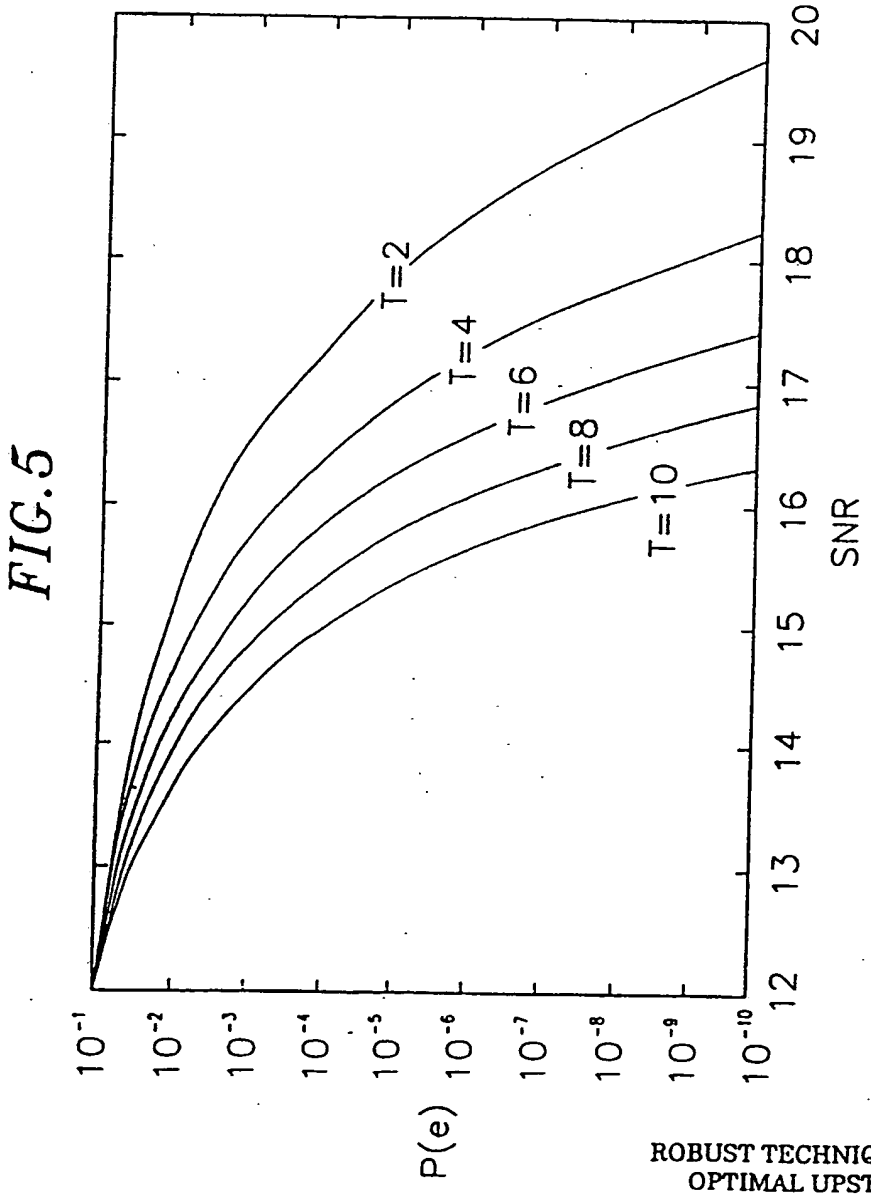
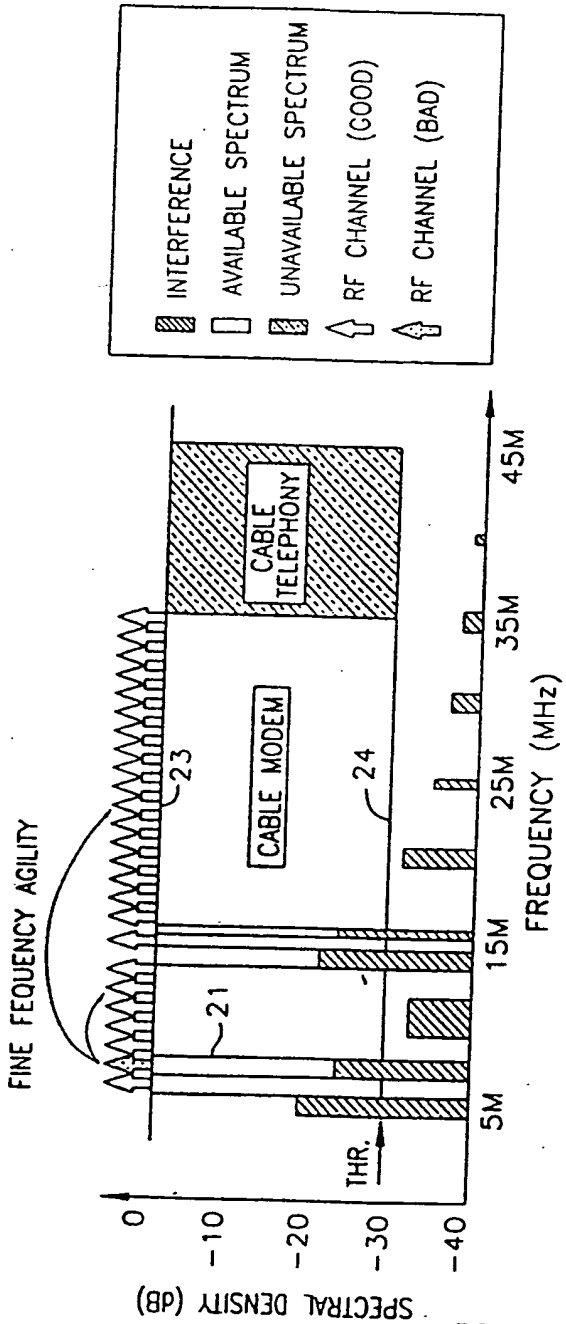


FIG.5

ROBUST TECHNIQUES FOR OPTIMAL UPSTREAM COMMUNICATION

FIG. 6



ROBUST TECHNIQUES FOR OPTIMAL UPSTREAM COMMUNICATION

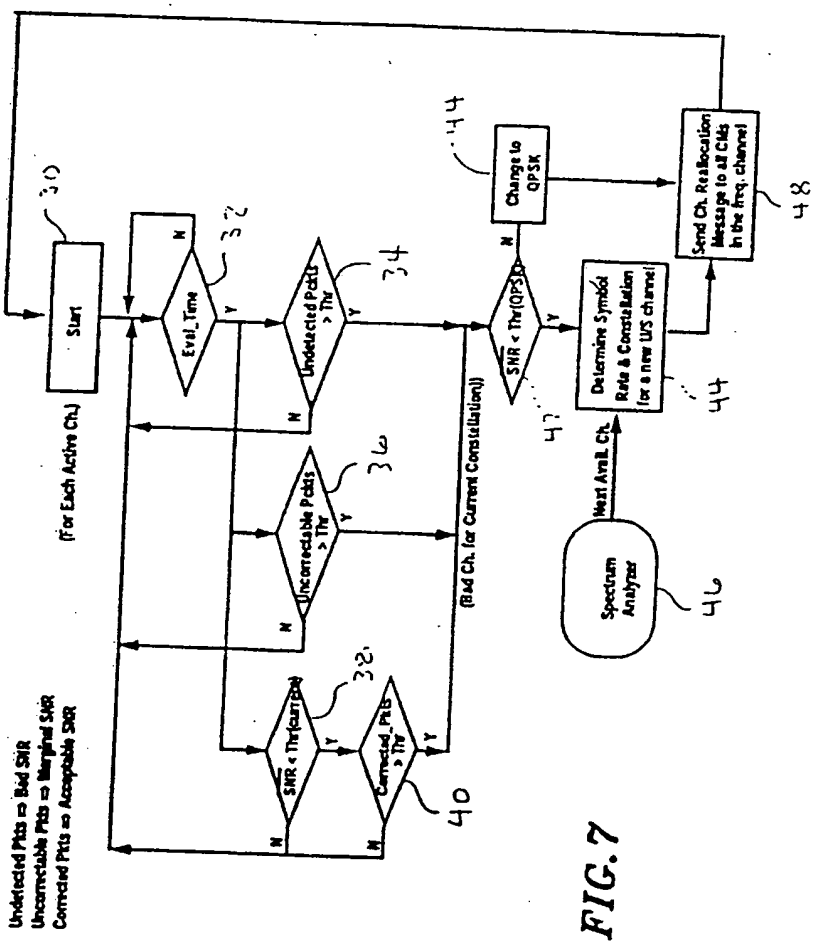


FIG. 7

ROBUST TECHNIQUES FOR OPTIMAL UPSTREAM COMMUNICATION

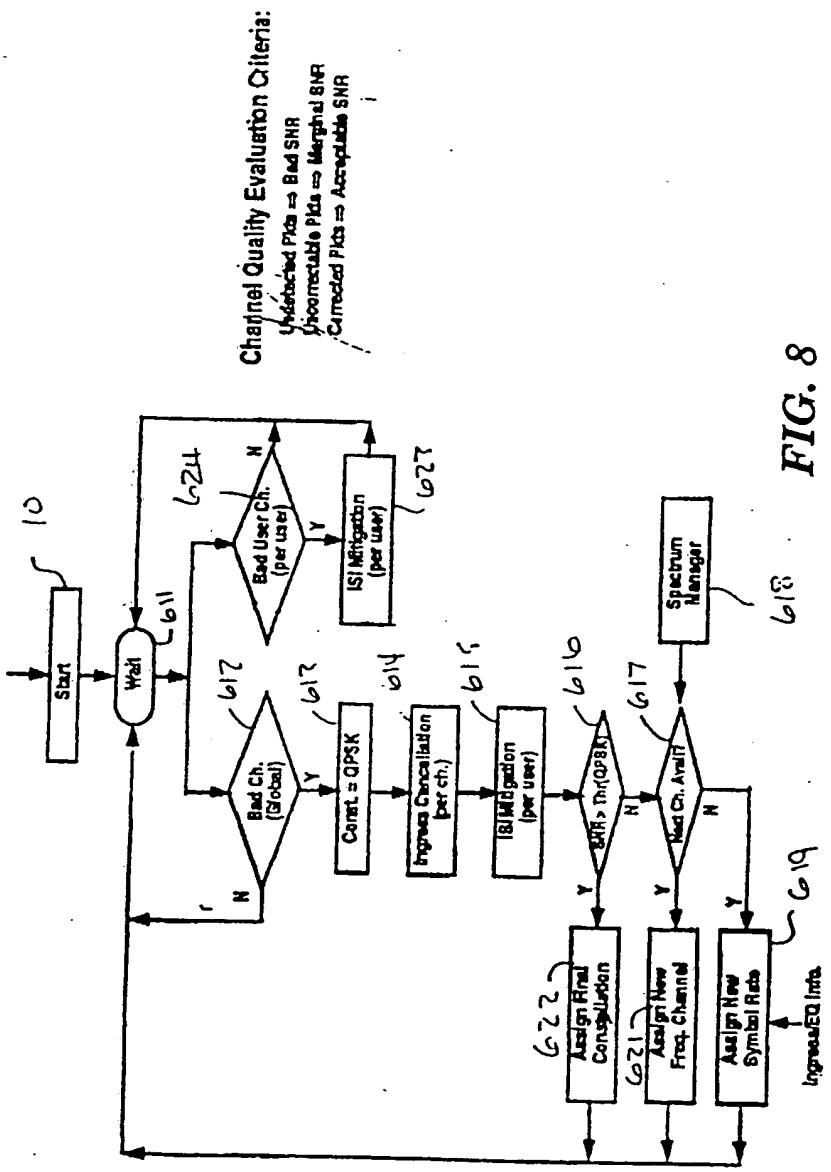


FIG. 8

ROBUST TECHNIQUES FOR OPTIMAL UPSTREAM COMMUNICATION

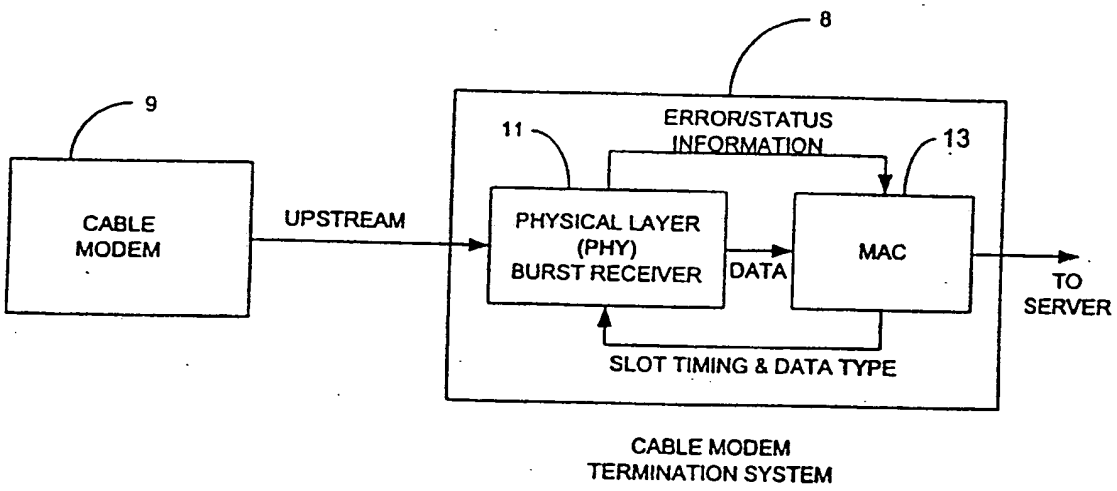


FIG. 1

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

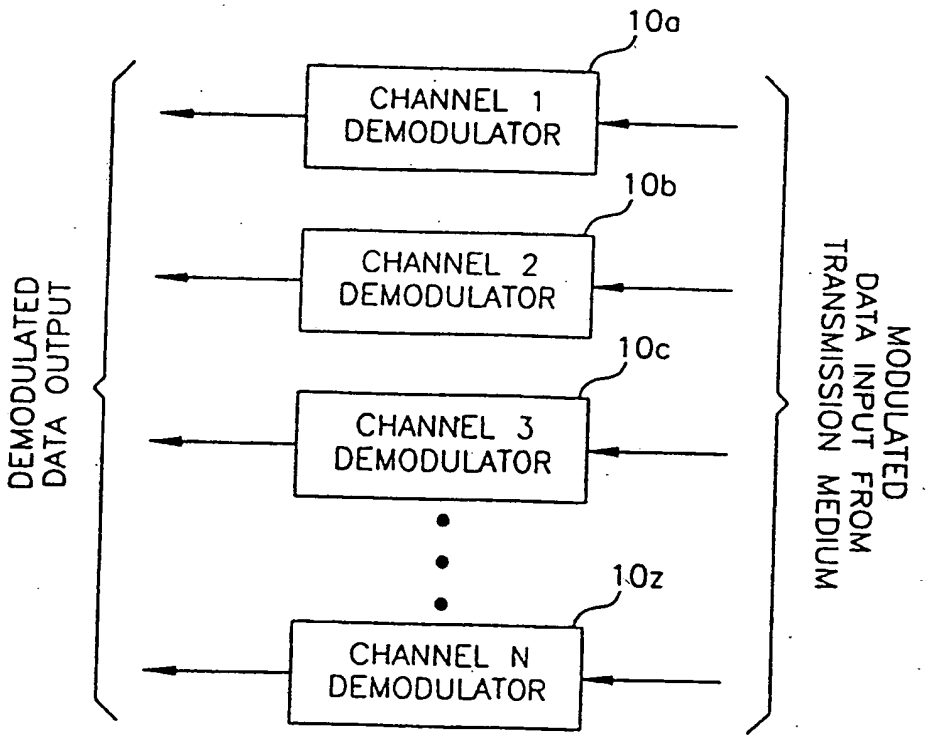


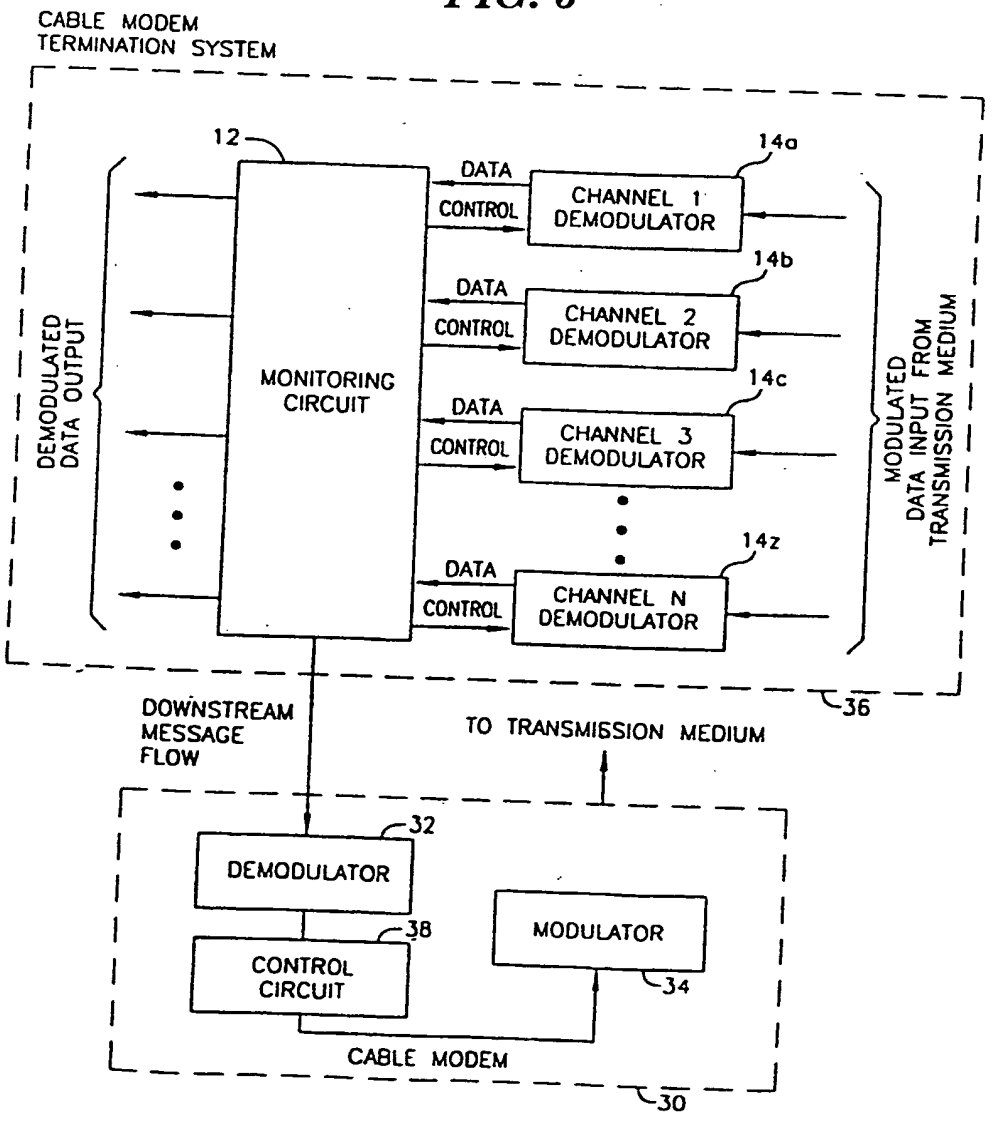
FIG. 2

(Prior Art)

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

FIG. 3



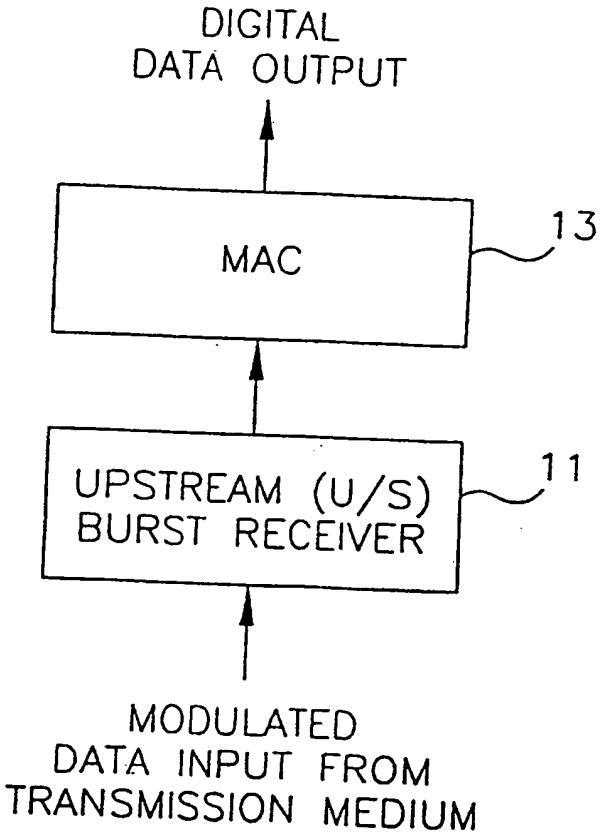


FIG. 4

(Prior Art)

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

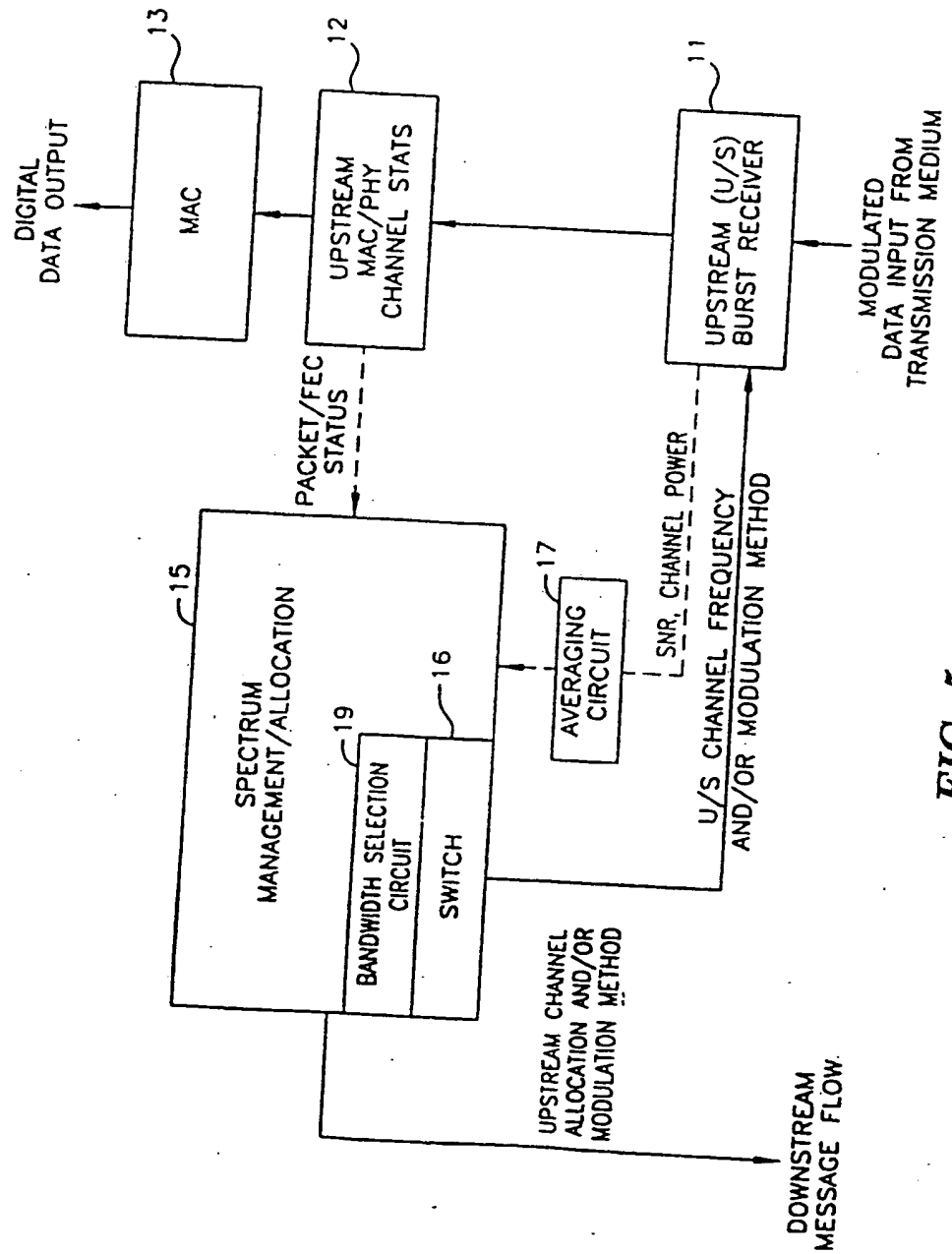


FIG. 5

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

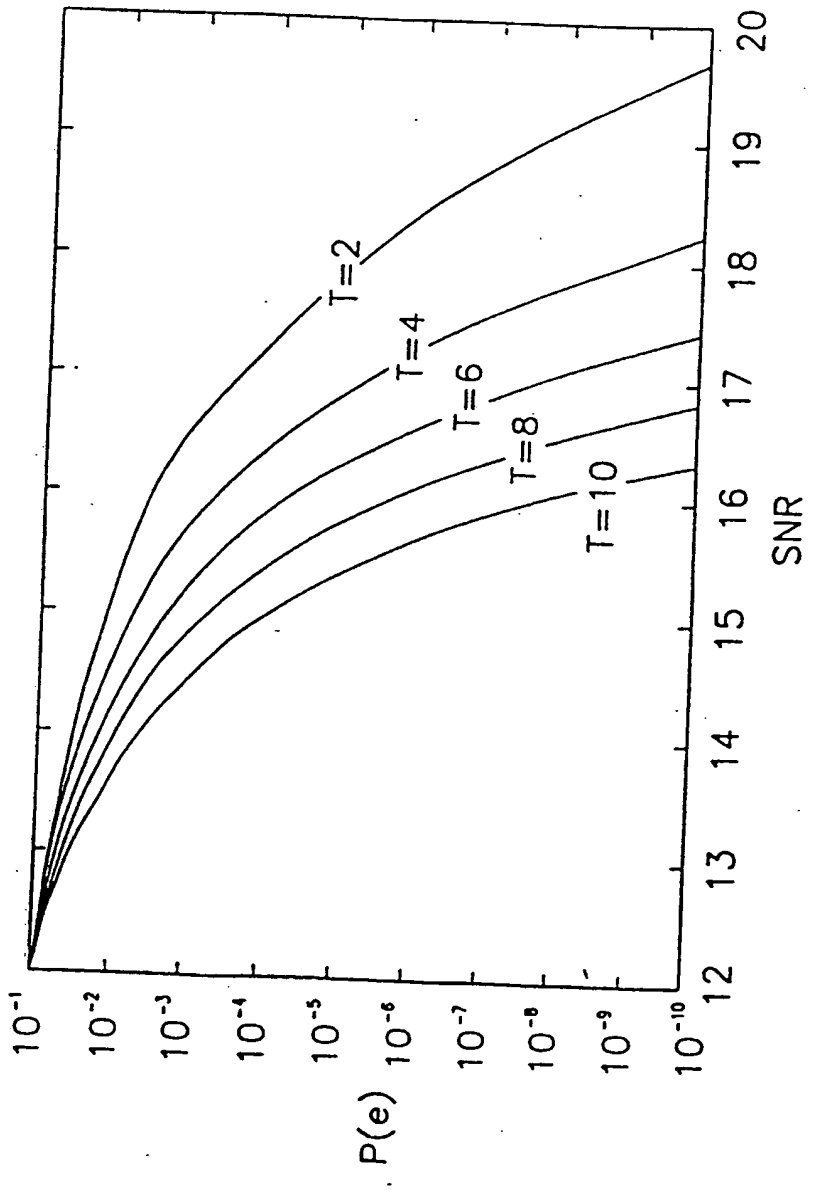


FIG. 6

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

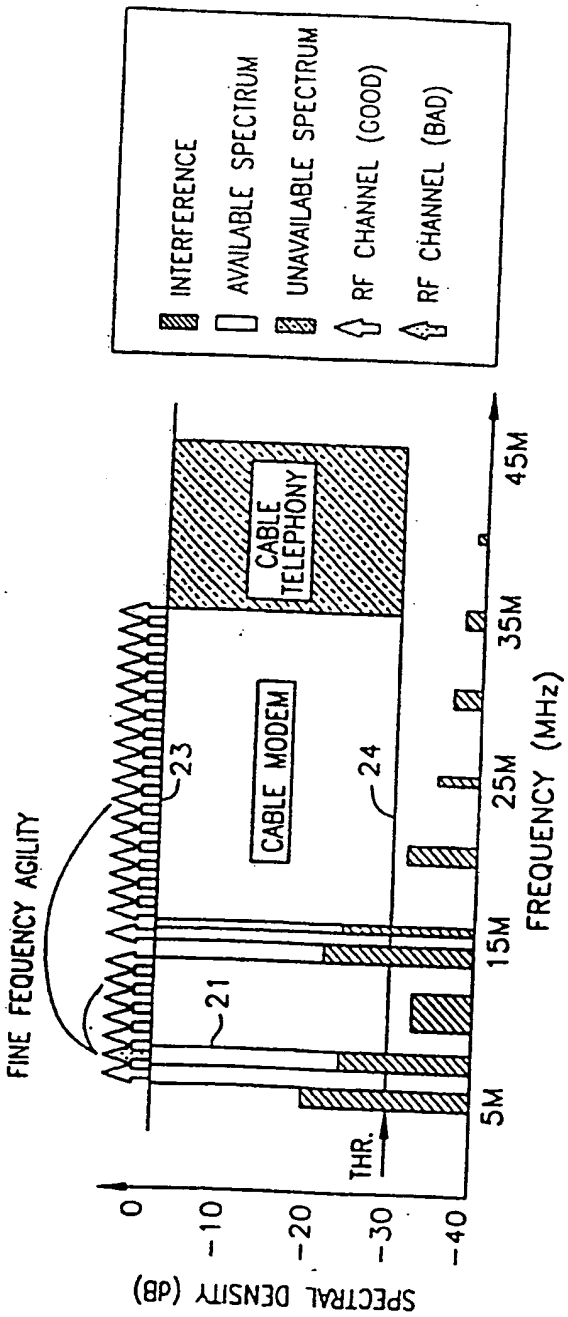


FIG. 7

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

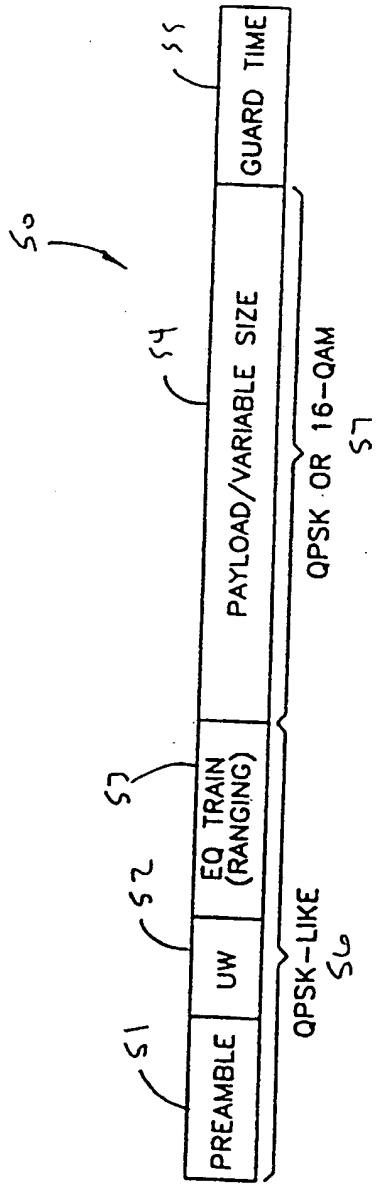


FIG. 7A

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

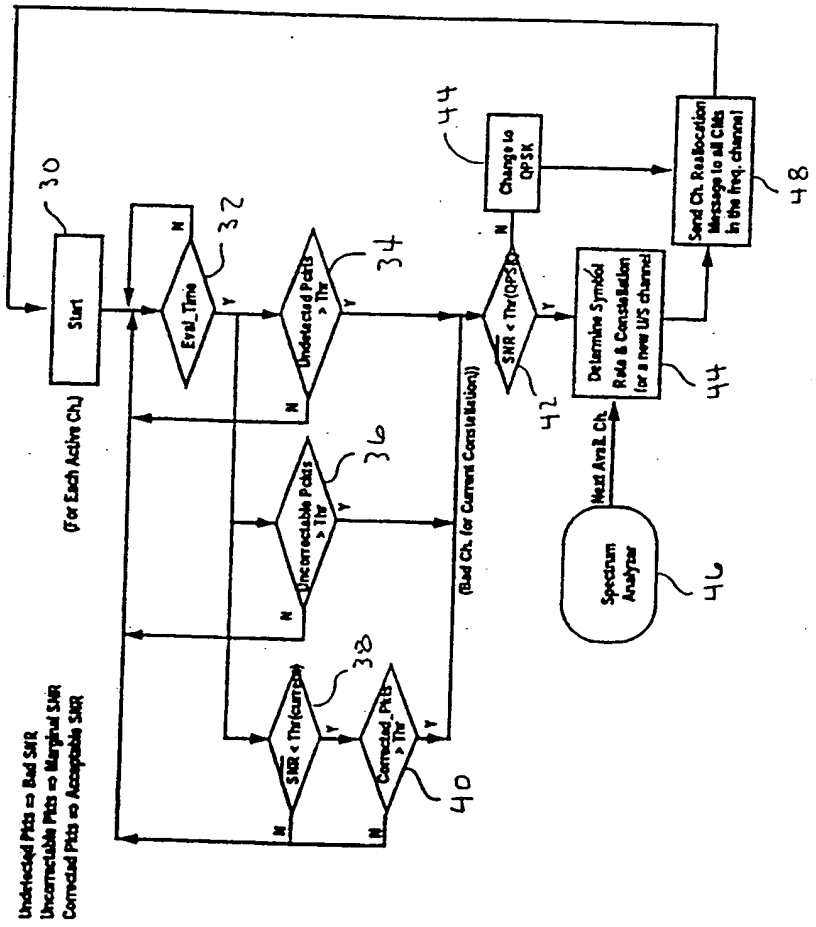


FIG. 8

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

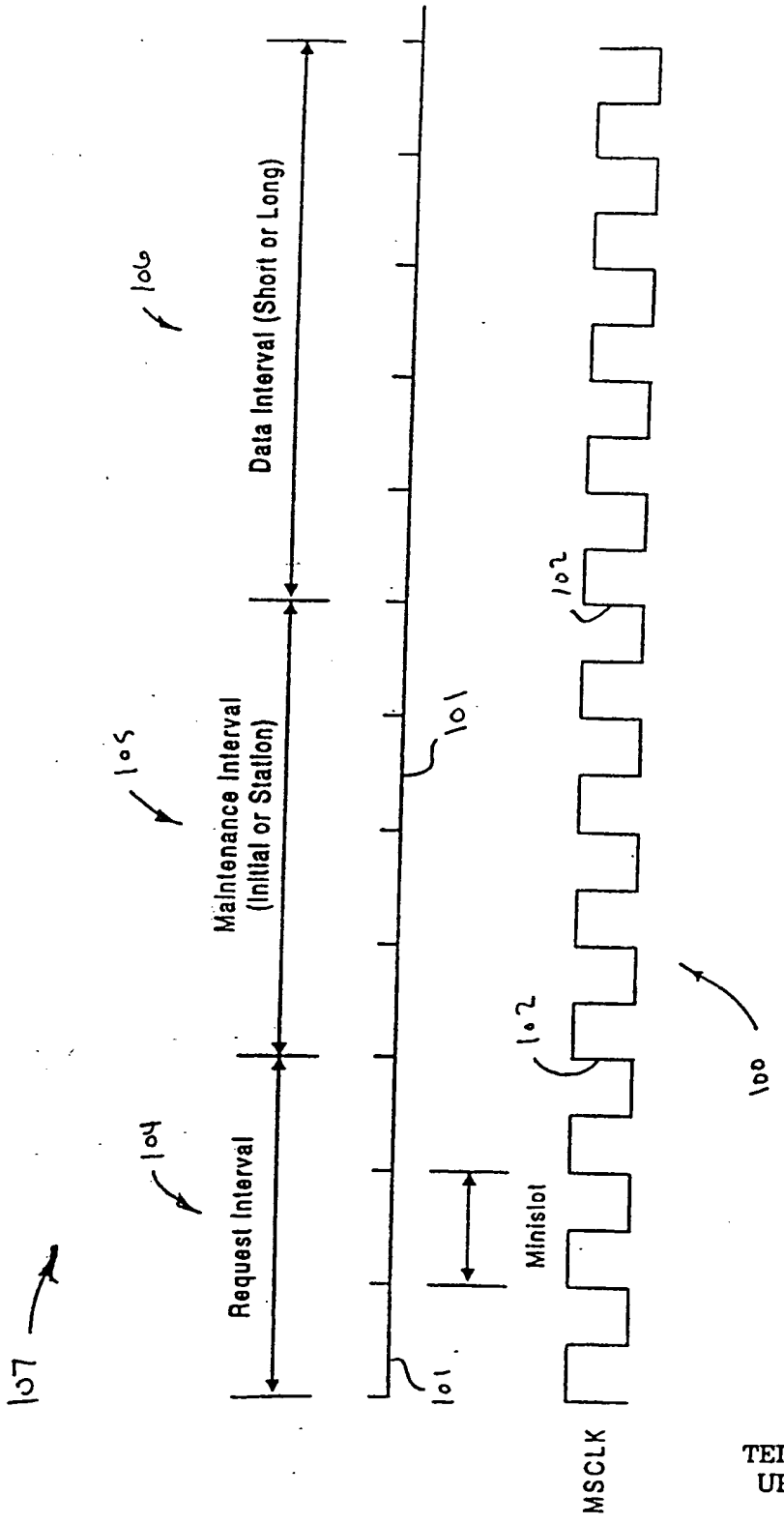


FIG. 9

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

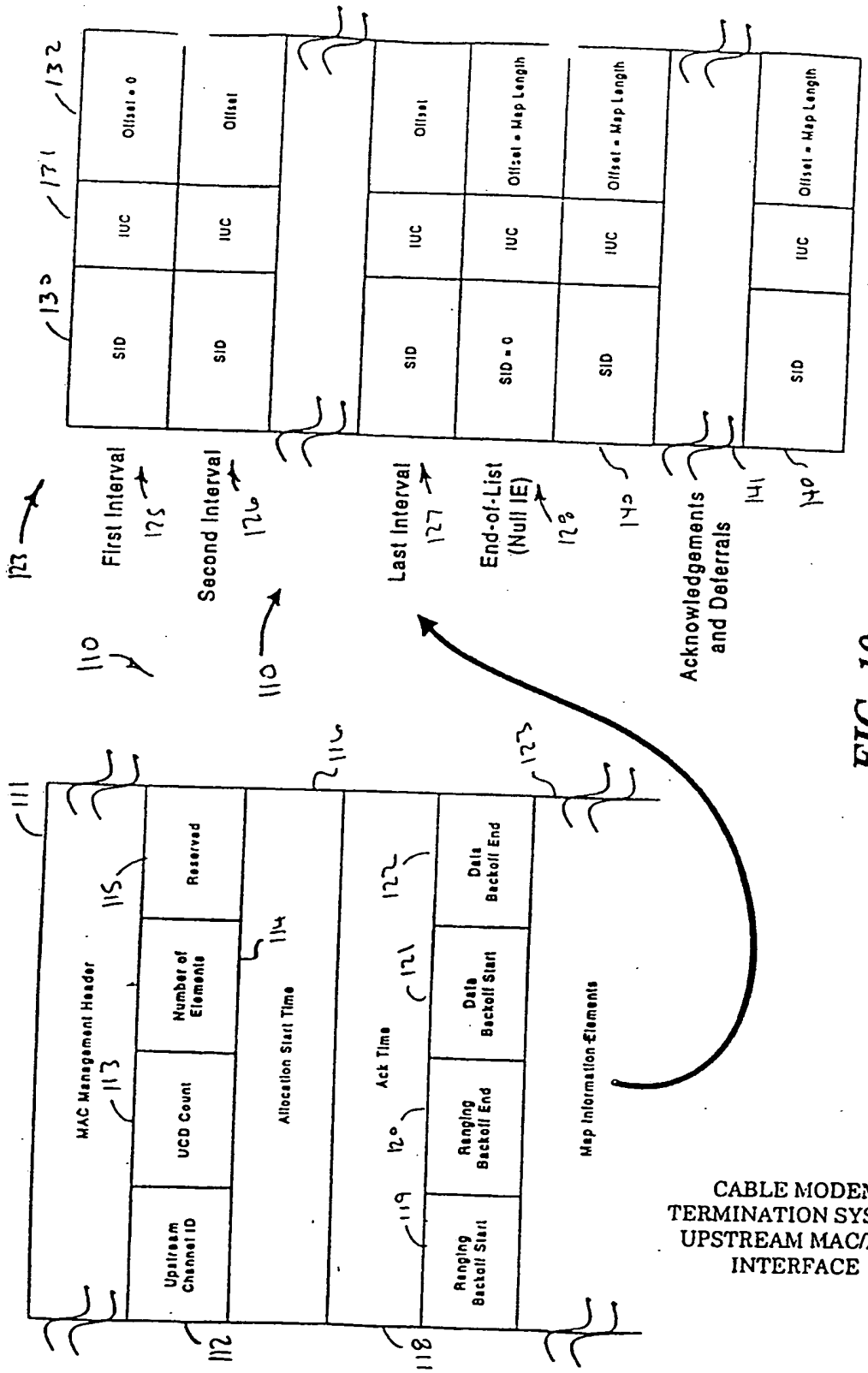

MAC Management Header
UCD Count
Upstream Channel ID
Number of Elements
Reserved
Allocation Start Time
Ack Time
Ranging Backoff Start
Ranging Backoff End
Data Backoff Start
Data Backoff End
Map Information Elements
SID
IUC
Offset = 0
Offset
Offset = Map Length
SID = 0
First Interval
Second Interval
Last Interval
End-of-List (Null IE)
Acknowledgements and Deferrals
CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

FIG. 10

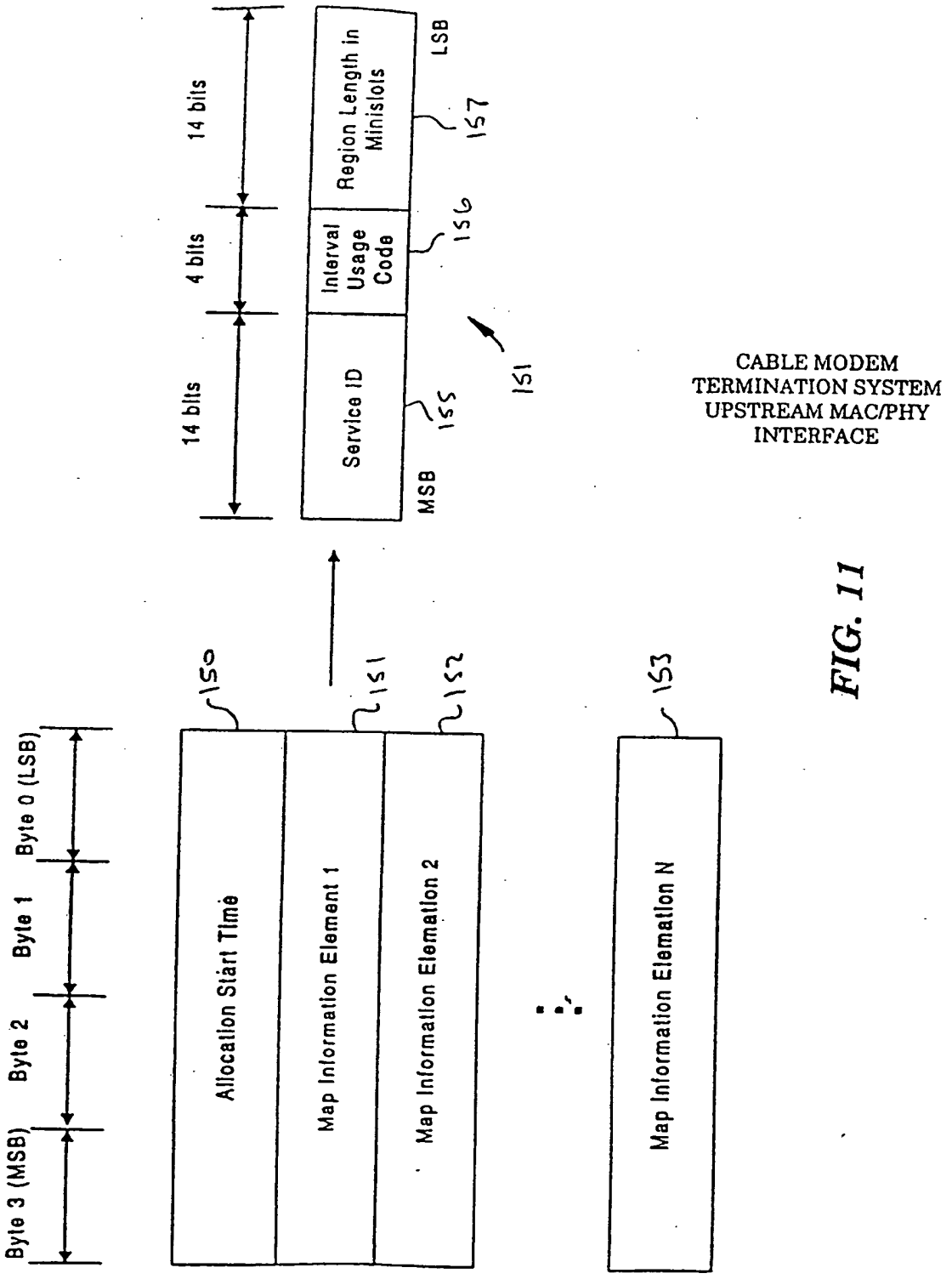

14 bits
4 bits
14 bits
Region Length in Minislots
LSB
157
Interval Usage Code
156
Service ID
155
MSB
151
CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE
150
151
152
153
Allocation Start Time
Map Information Element 1
Map Information Elemation 2
Map Information Elemation N
Byte 0 (LSB)
Byte 1
Byte 2
Byte 3 (MSB)

FIG. 11

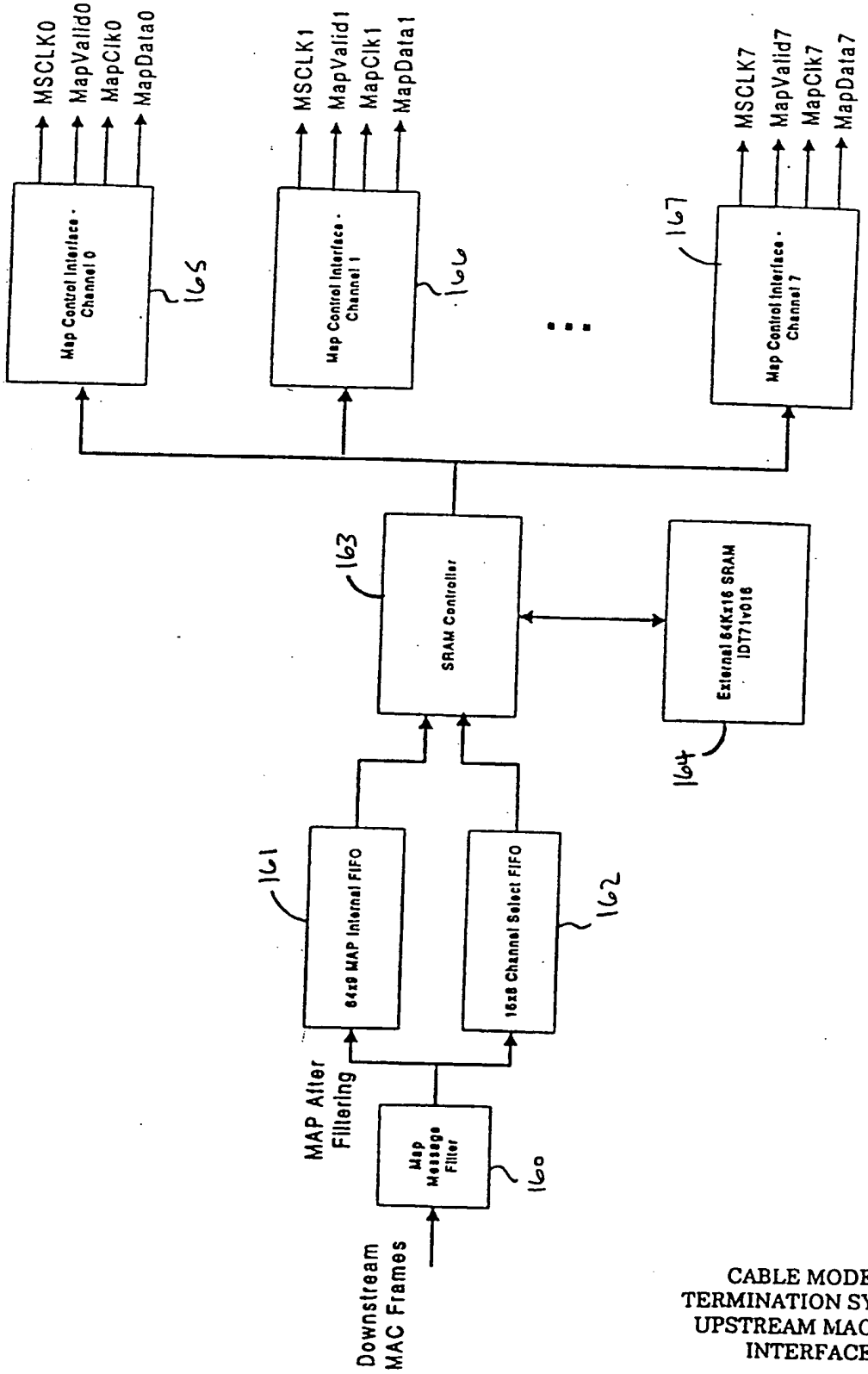


FIG. 12

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

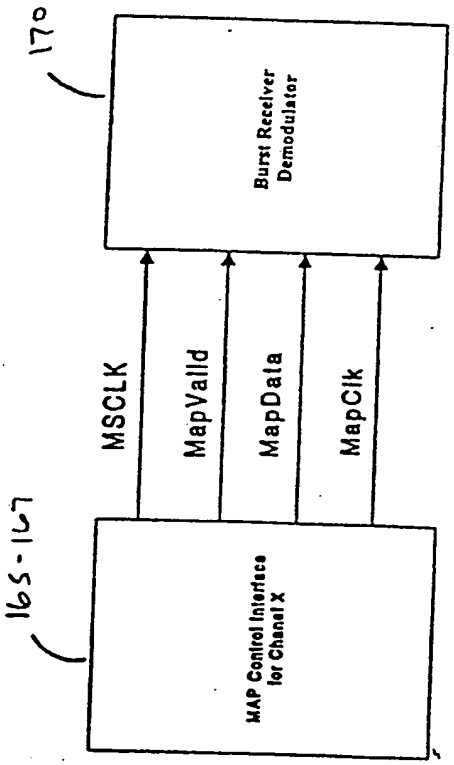


FIG. 13

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

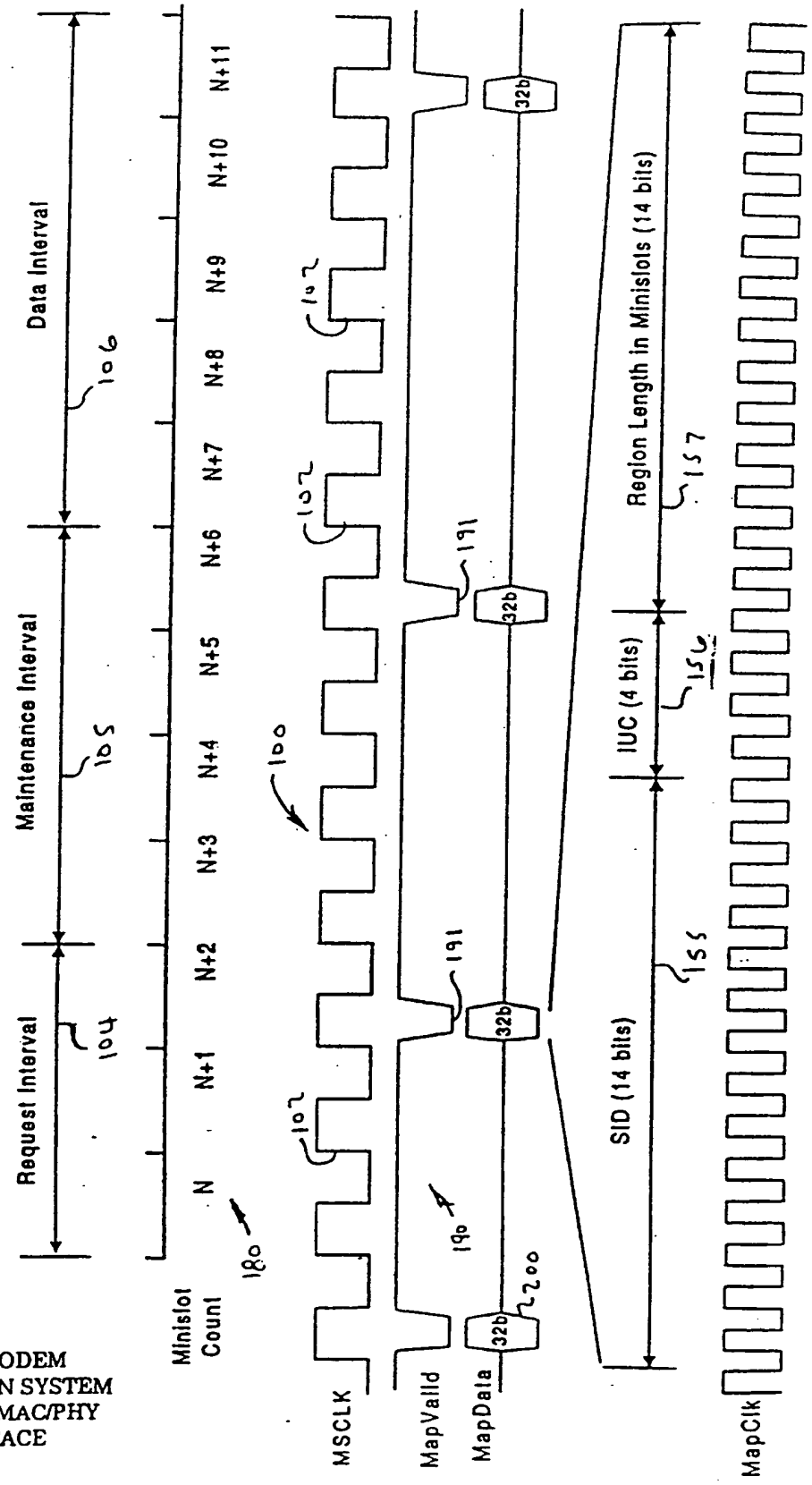


FIG. 14

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

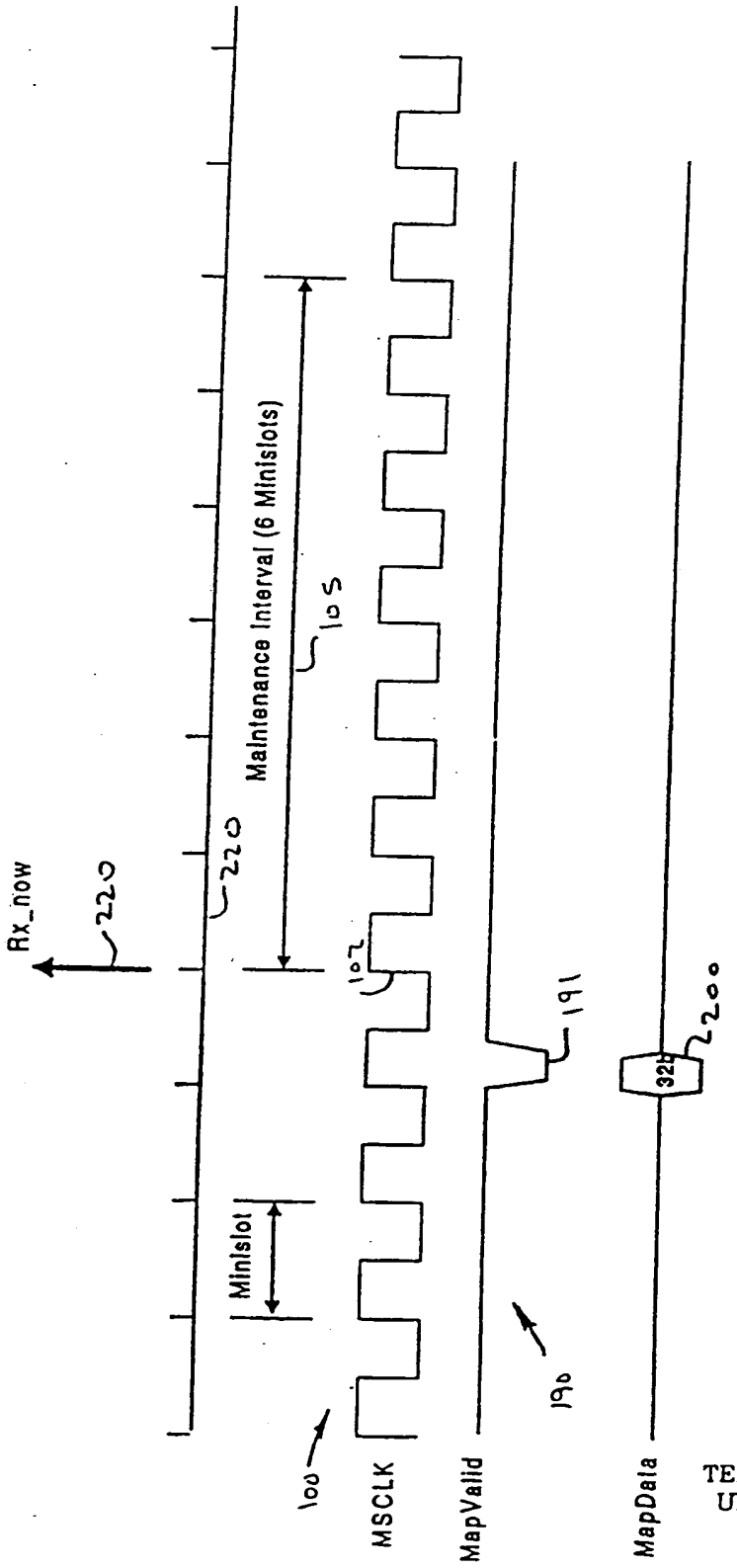


FIG. 15

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

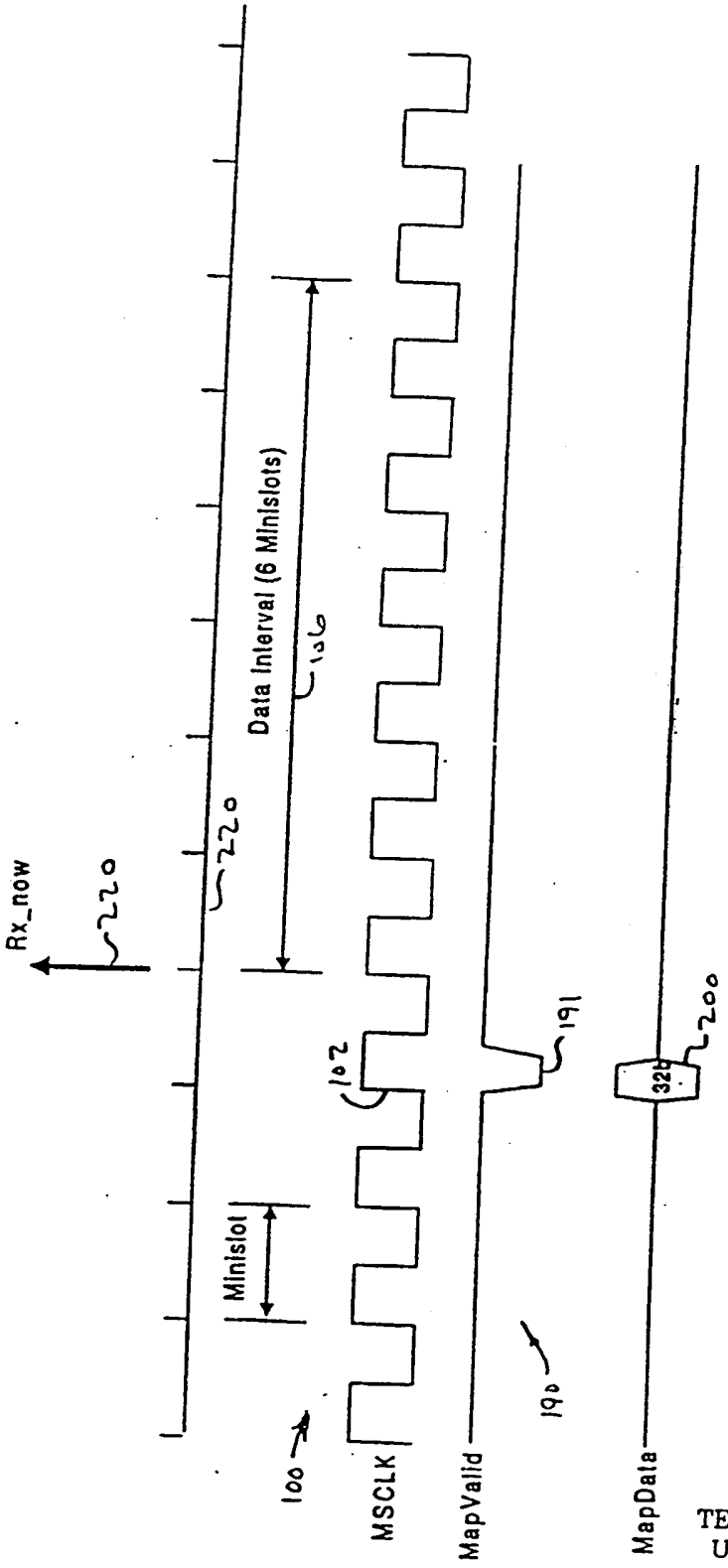


FIG. 16

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

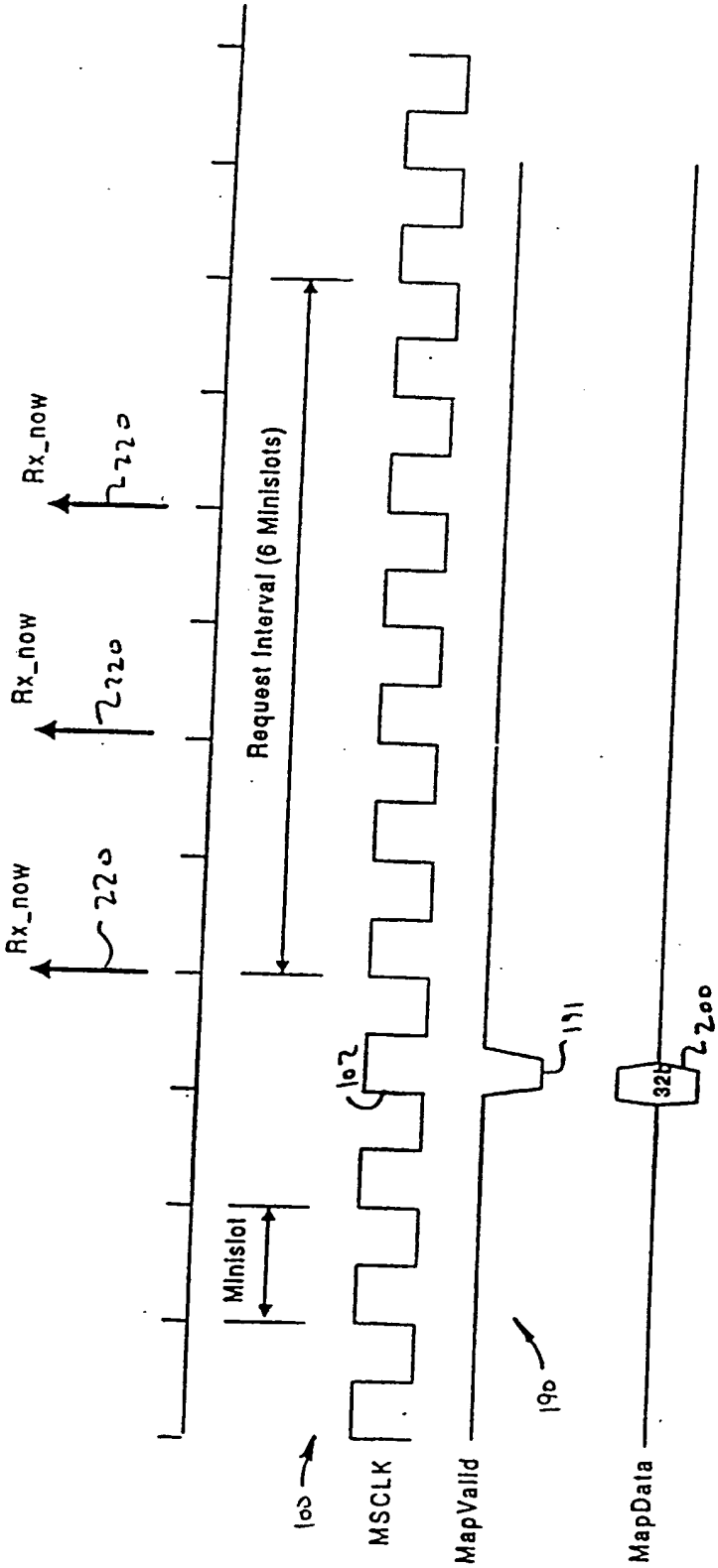


FIG. 17

* In this example, it is assumed that each request message requires two minislots to transmit

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

Rng. Offset 7 bytes

Status 2 bytes	Timestamp 4 bytes	Ch. ID 1 byte	SID 2 bytes	Pwr. 2 bytes	Freq. 2 bytes	Time 3 bytes

FIG. 18

Rng. Offset 7 bytes

Status 2 bytes	Timestamp 4 bytes	Ch. ID 1 byte	SID 2 bytes	Pwr. 2 bytes	Freq. 2 bytes	Time 3 bytes	Equalizer Coeffs. 32 bytes

FIG. 19

Based on the Status bytes [7:5] bits, the following statistics are kept using counters.

Slot Definition	Statistics	Calculation
Data	1. Number of slots 2. Number of Slots with power but no data 3. Number of slots with bad data 4. Number of Good data-slots 5. Total number of FEC Blocks 6. Number of FEC blocks with correctable errors. 7. Number of uncorrectable FEC blocks	No UW UW and (Bad FEC or Bad HEC) UW and Good HEC
Request (Contention)	1. Number of requests received 2. Number of collided requests 3. Number of corrupted requests	No UW No UW or Bad FEC or Bad HEC
Request/Data (Contention)	1. Number of packets received 2. Number of collided packets 3. Number of corrupted packets	No UW No UW or Bad FEC or Bad HEC
Ranging	1. Number of ranging messages received 2. Number of collided ranging messages received 3. Number of corrupted ranging messages	No UW No UW or Bad FEC or Bad HEC

FIG. 20

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

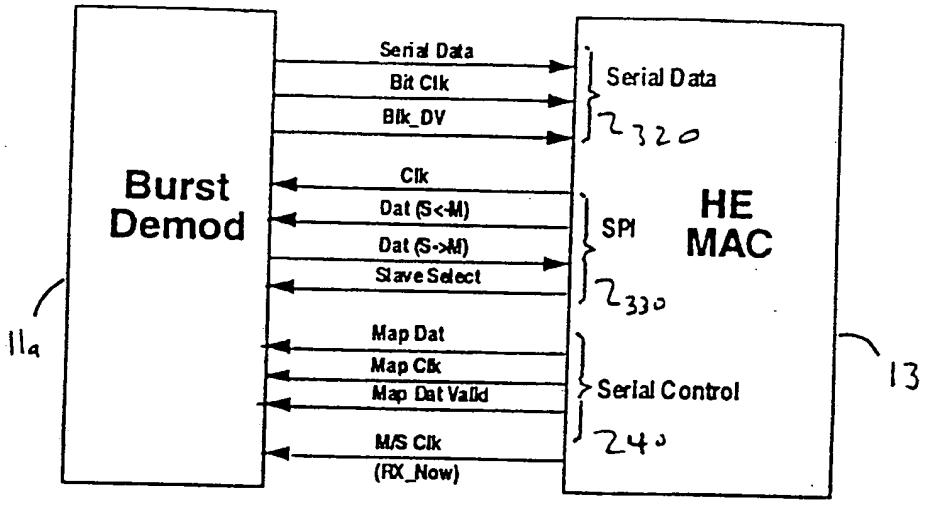


FIG. 21

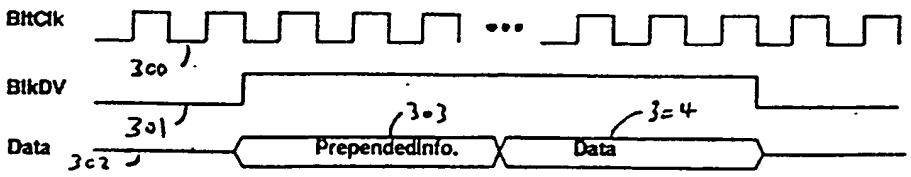


FIG. 22

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

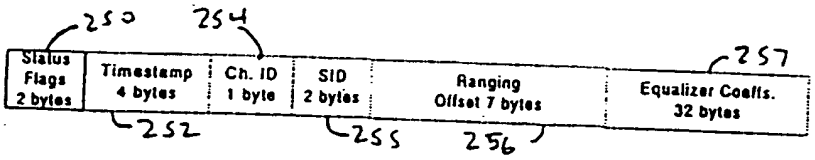


FIG. 23

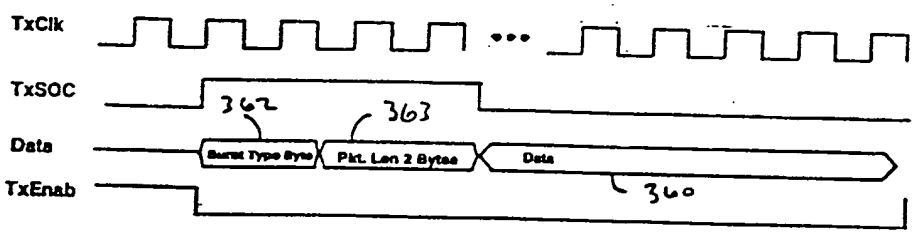


FIG. 24

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

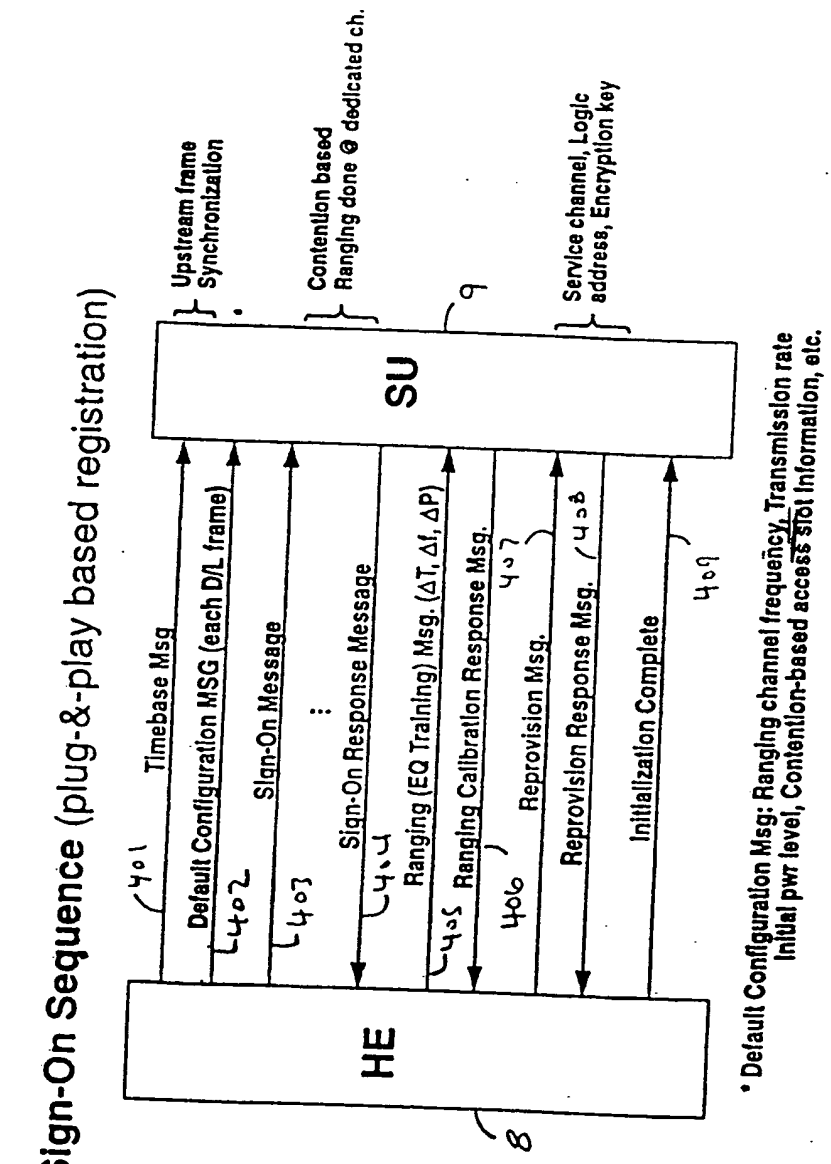
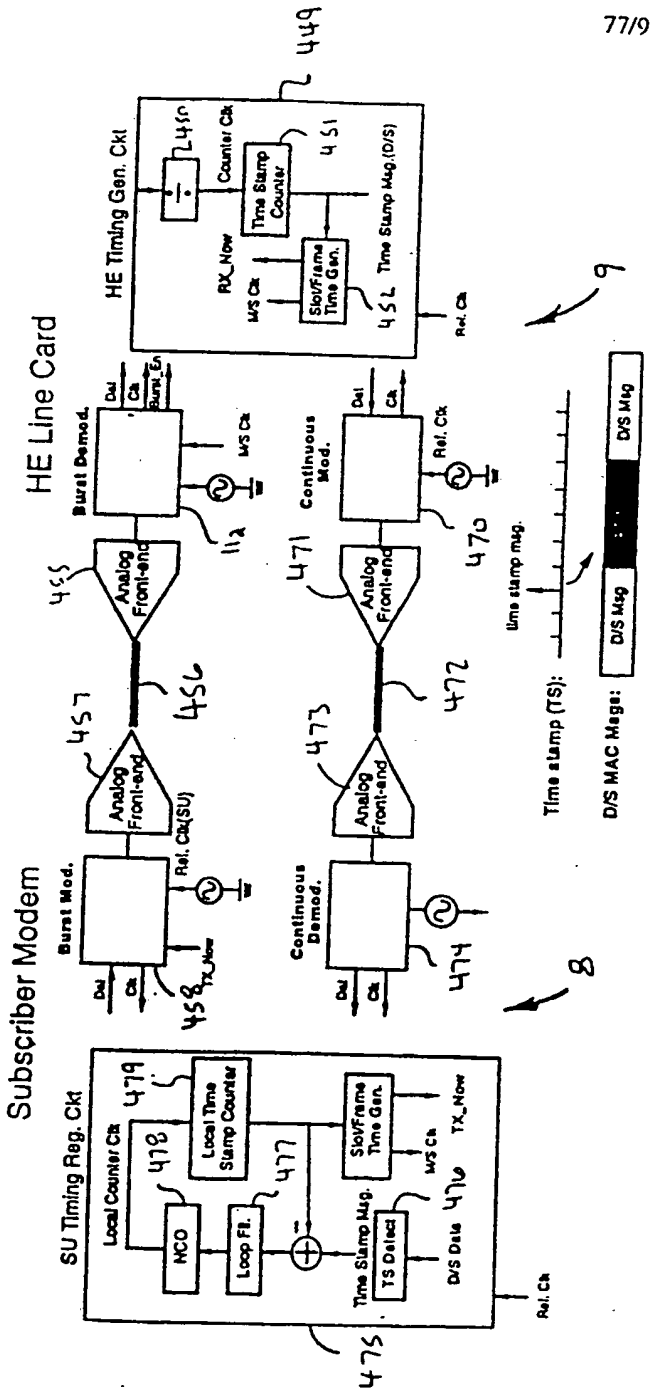


FIG. 25

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE



- MAC framing and PHY framing are decoupled
- Upstream frame synchronization based on time stamp messages

FIG. 26

CABLE MODEM TERMINATION SYSTEM UPSTREAM MAC/PHY INTERFACE

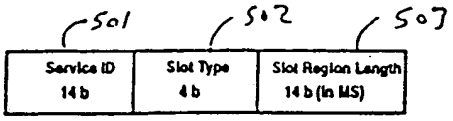


FIG. 27

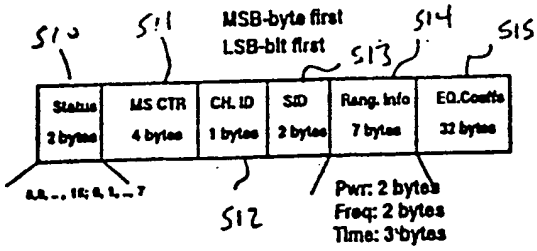


FIG. 28

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

Bit Field	Definition if Bit[11]=1	Definition if Bit[11]=0
Bit[15:12]	MCNS IUC	Reserved
Bit [11]	1: indicates 1st block of transmission	0: indicates not 1st block of transmission
Bit [10]	1: indicates last block of transmission	1: indicates last block of transmission
Bit [9]	1: indicates Ranging required	Reserved
Bit [8]	Reserved	Reserved
Bit [7:5]	000: FEC OK 001: Correctable FEC Error 010: uncorrectable FEC error 011: no Unique word detected 100: collided packet 101: no energy 110: packet length violation	000: FEC OK 001: Correctable FEC Error 010: uncorrectable FEC error 011: no Unique word detected 100: collided packet 101: no energy 110: packet length violation
Bit [4]	1: Valid Minislot count prepended	Reserved
Bit [3]	1: Valid Channel ID prepended	Reserved
Bit [2]	1: Valid SID prepended	Reserved
Bit [1]	1: Ranging Info prepended	Reserved
Bit [0]	1: Equalizer coefficients prepended	Reserved

FIG. 29

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

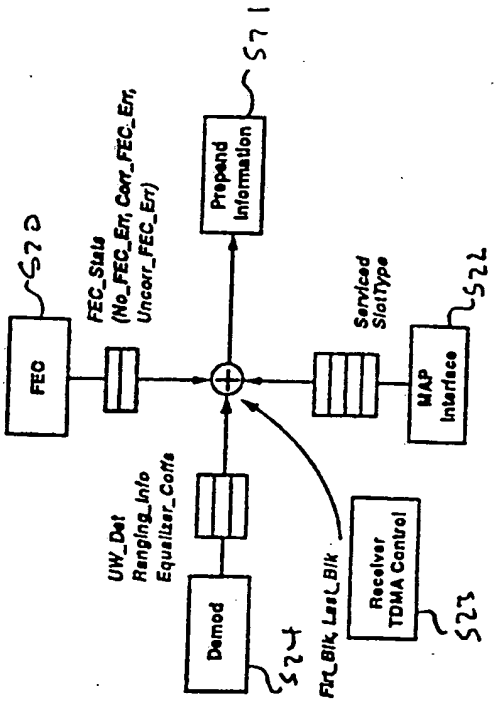


FIG. 30

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

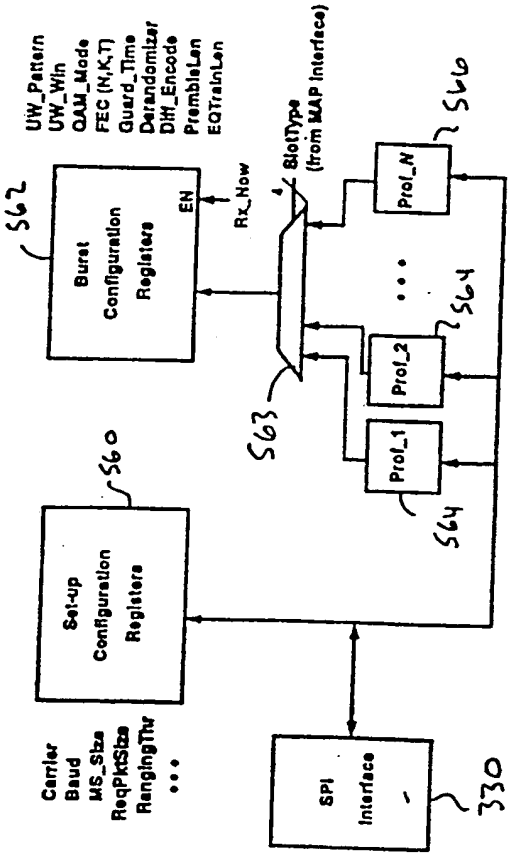


FIG. 31

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

CABLE MODEM
TERMINATION SYSTEM
UPSTREAM MAC/PHY
INTERFACE

FIG. 32

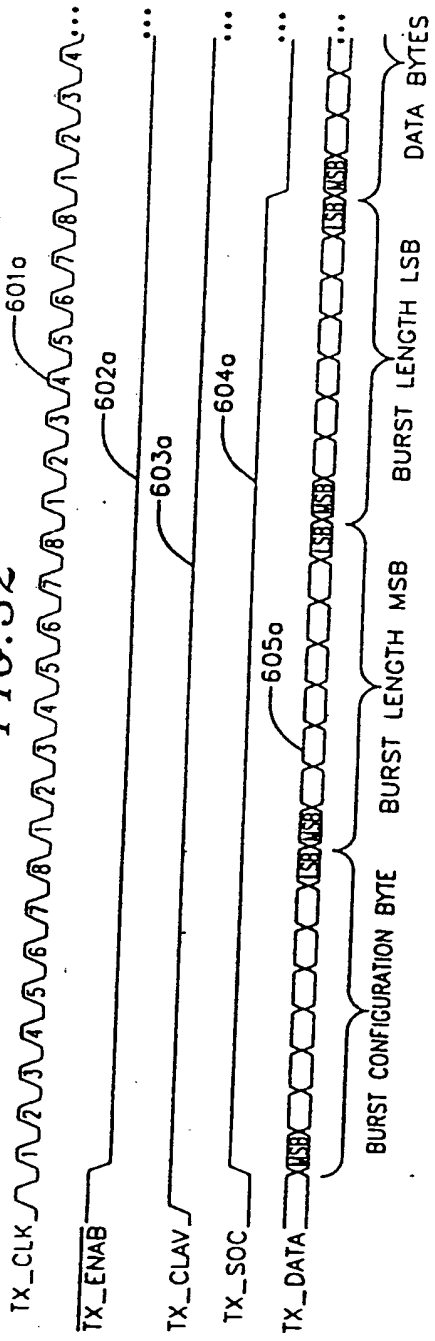


FIG. 33

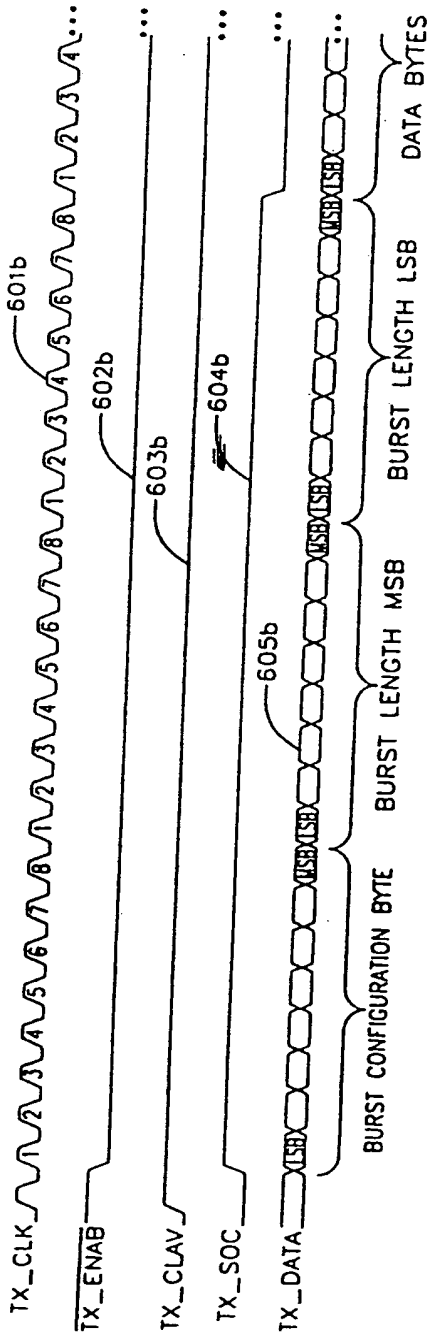
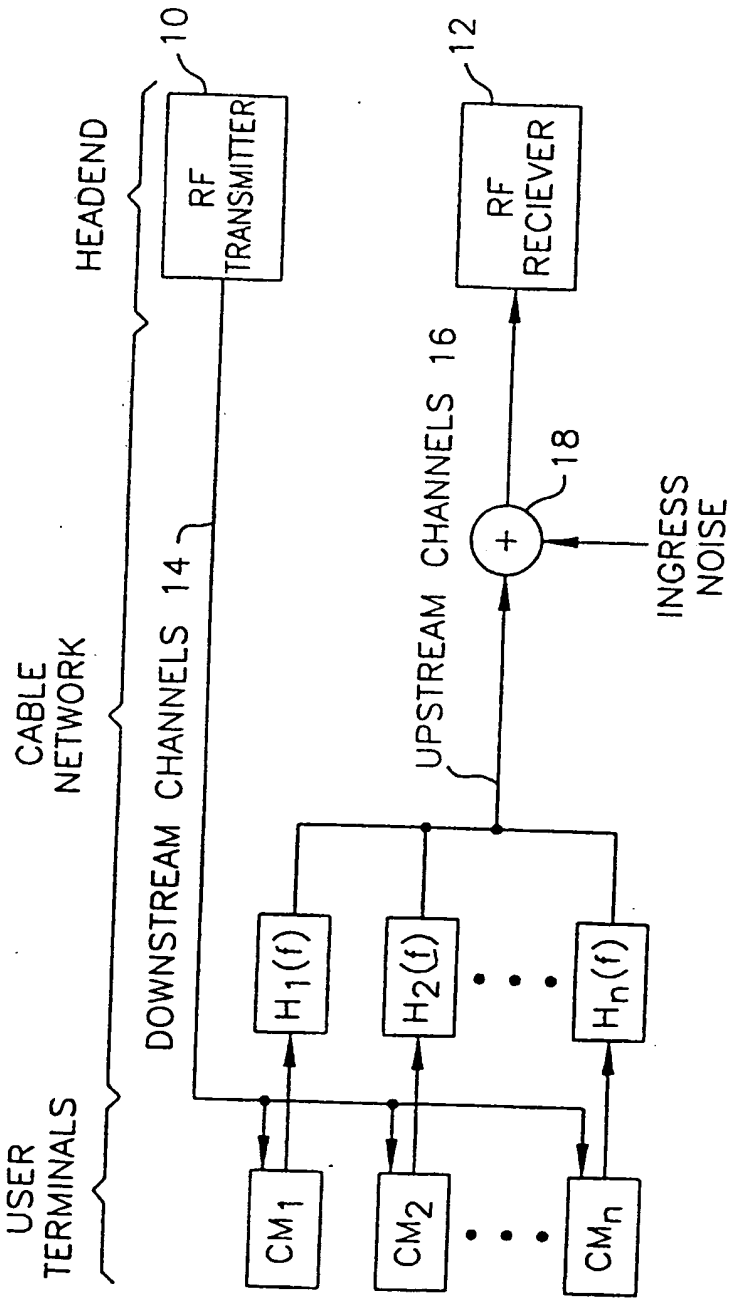


FIG. 1


HEADEND
10
RF TRANSMITTER
12
RF RECIEVER
CABLE NETWORK
DOWNSTREAM CHANNELS 14
UPSTREAM CHANNELS 16
18
INGRESS NOISE
USER TERMINALS
$H_1(f)$
$H_2(f)$
$H_n(f)$
CM_1
CM_2
CM_n

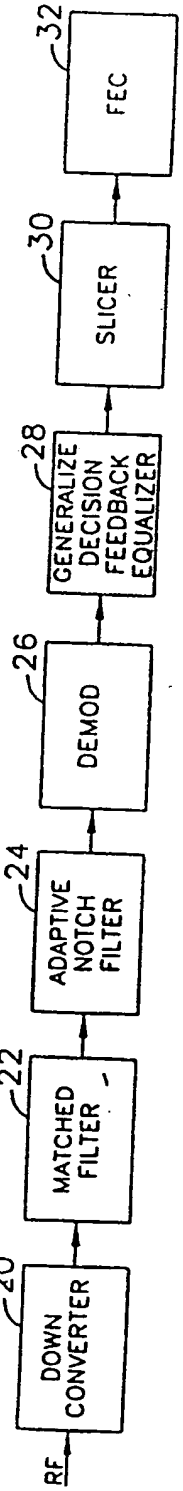

RF
20
DOWN CONVERTER
22
MATCHED FILTER
24
ADAPTIVE NOTCH FILTER
26
DEMOD
28
GENERALIZE DECISION FEEDBACK EQUALIZER
30
SLICER
32
FEC

FIG.2

FIG.3

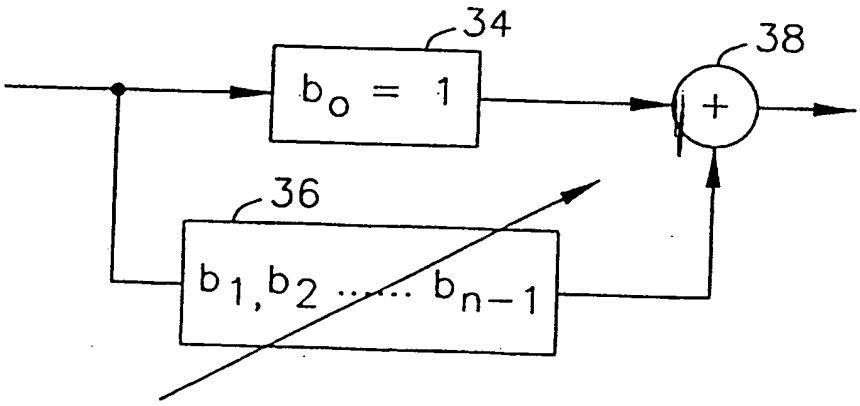
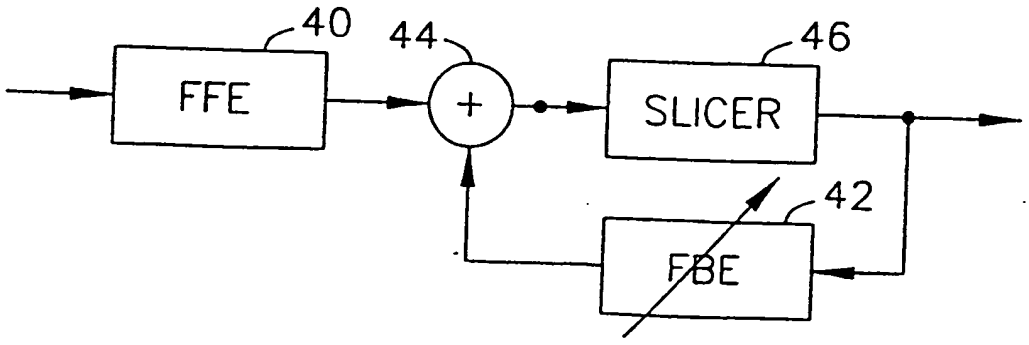


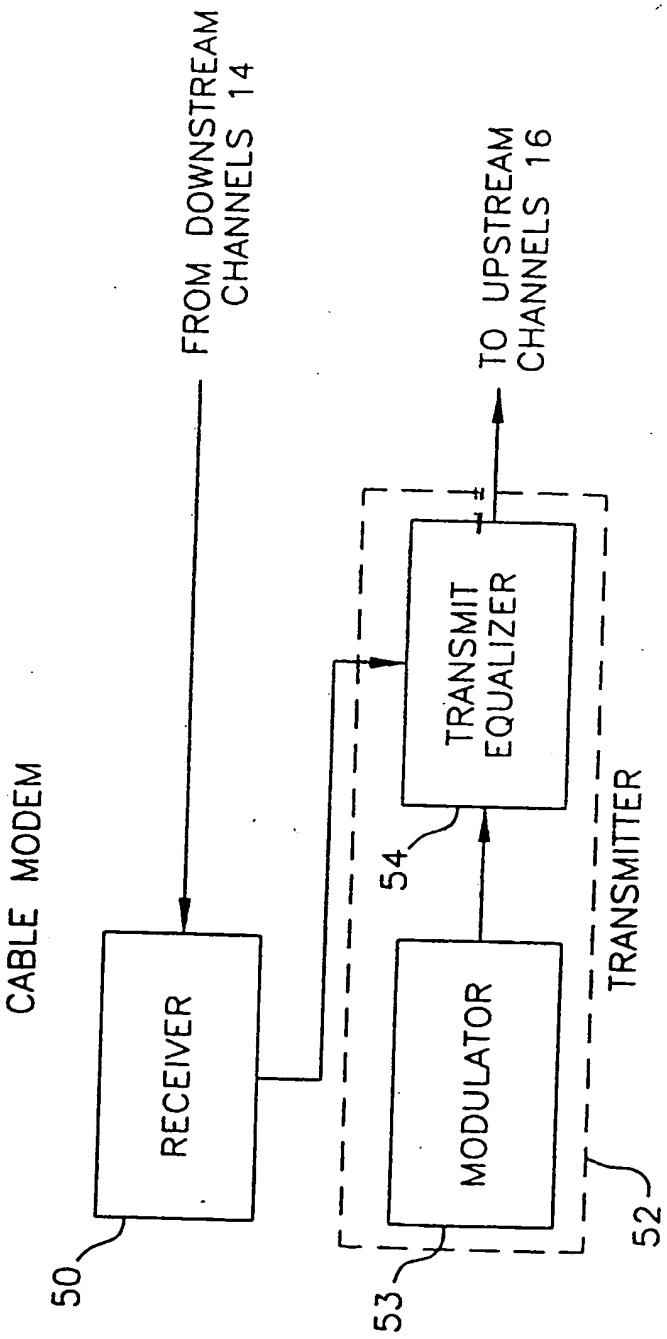
FIG.4



METHOD AND APPARATUS FOR REDUCING NOISE IN A BIDIRECTIONAL CABLE TRANSMISSION SYSTEM

METHOD AND APPARATUS FOR REDUCING NOISE IN A BIDIRECTIONAL CABLE TRANSMISSION SYSTEM

FIG. 5



METHOD AND APPARATUS FOR REDUCING NOISE IN A BIDIRECTIONAL CABLE TRANSMISSION SYSTEM

FIG. 6

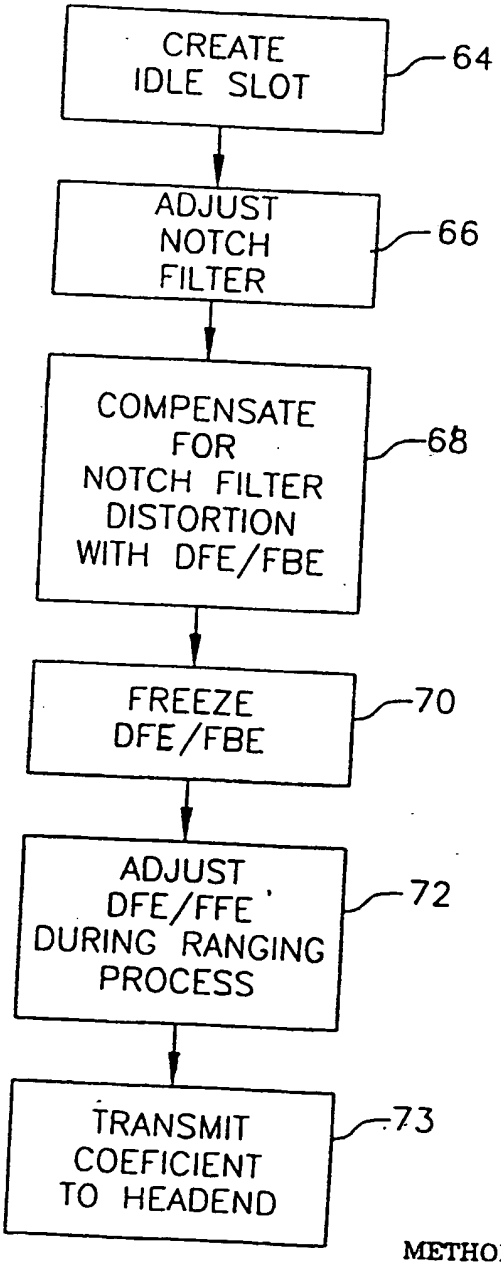


FIG. 7

METHOD AND APPARATUS FOR REDUCING NOISE IN A BIDIRECTIONAL CABLE TRANSMISSION SYSTEM

FIG. 8A

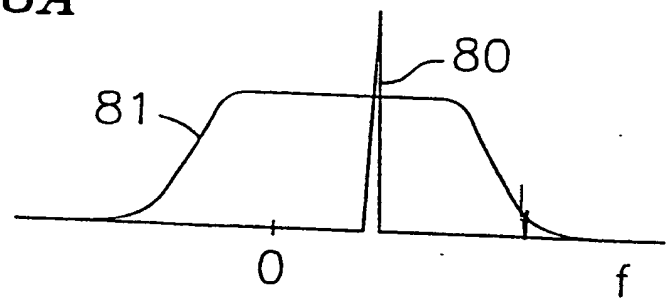


FIG. 8B

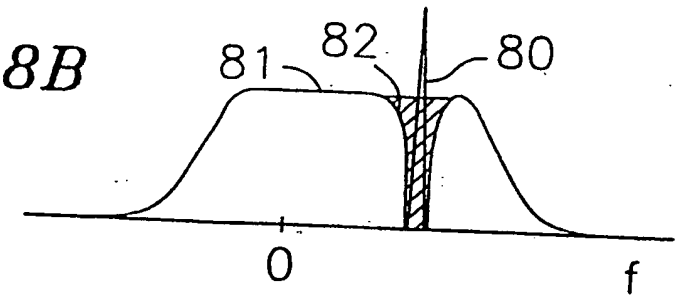
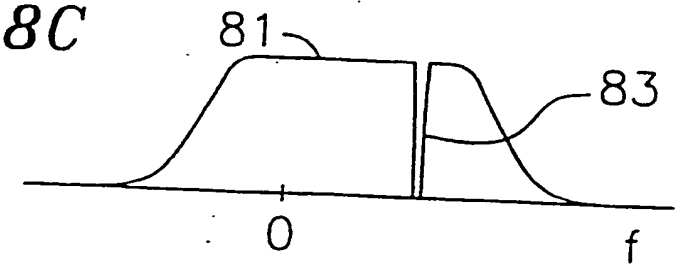


FIG. 8C



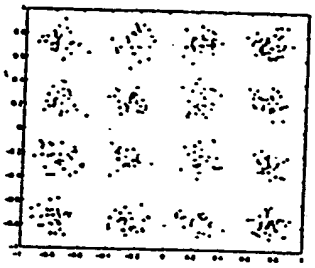


Fig. 9A

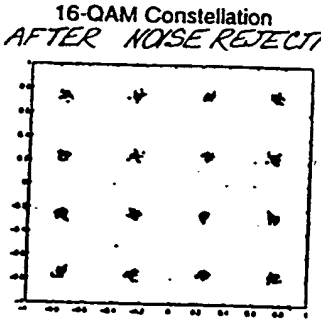


Fig. 9B

METHOD AND APPARATUS FOR REDUCING NOISE IN A BIDIRECTIONAL CABLE TRANSMISSION SYSTEM

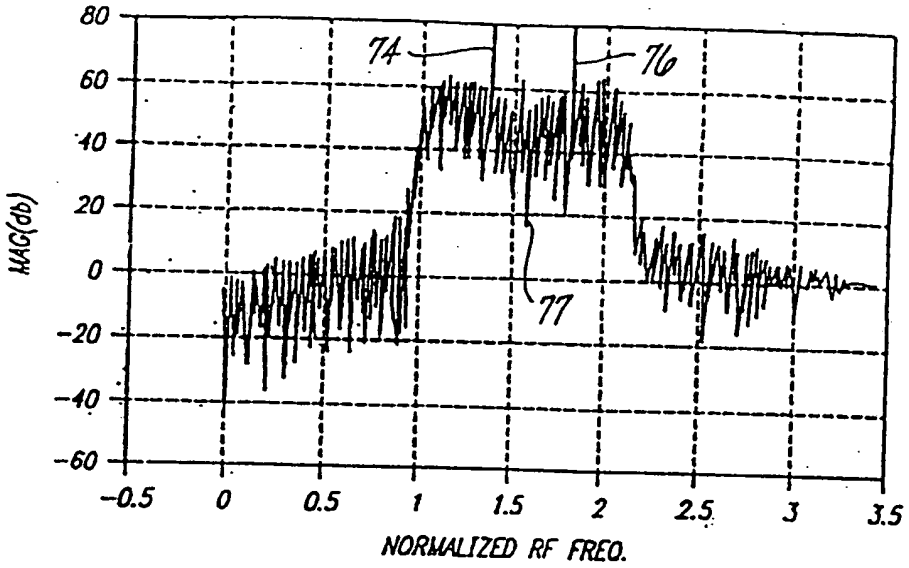


Fig. 10A

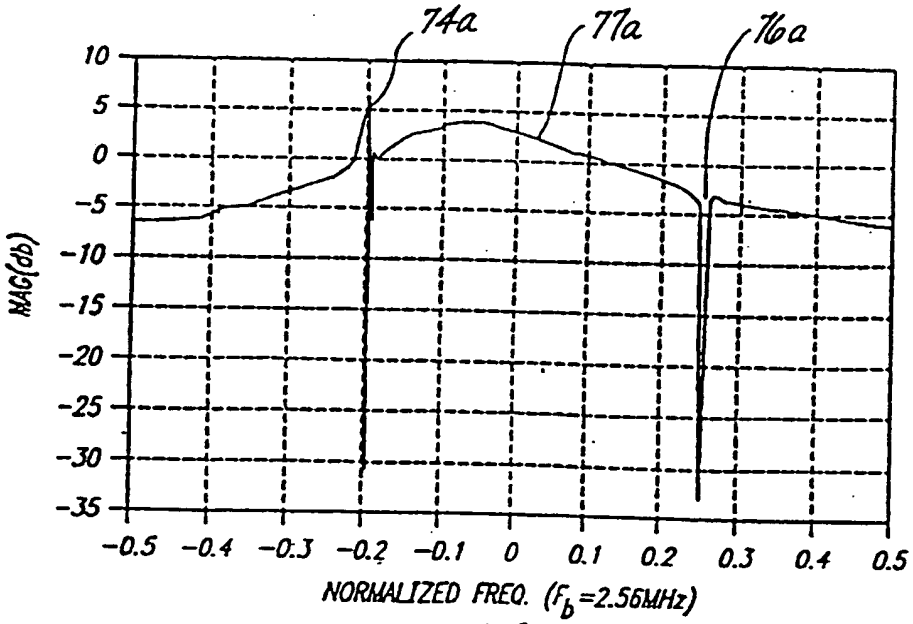


Fig. 10B

METHOD AND APPARATUS FOR REDUCING NOISE IN A BIDIRECTIONAL CABLE TRANSMISSION SYSTEM

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